DAVICOM Semiconductor, Inc.

DM8606AF

6-Port Fast Ethernet
Single Chip Switch Controller

DATA SHEET

Preliminary
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Chapter 1 Product Overview

1.1 Overview

The DM8606AF is a high performance, low cost, highly integrated (Controller, PHY and Memory) four-port 10/100 Mbps TX/FX plus two 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex. The DM8606AF is intended for applications to stand alone bridge for low cost SOHO markets such as 5Port, Router applications. The 2nd MAC can be configured as PCS type MII with 10/100 PHY integrated.

DM8606AF provides the most advance functions such as: **802.1p(Q.O.S.), 802.1q(VLAN), Port MAC address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra MII port** functions to meet customer requests on Switch demand.

The DM8606AF also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffers are full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the DM8606AF will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in SRAM used for the packet buffer and address learning table is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

DM8606AF also supports priority features by Port-Base, VLAN and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN are also supported.

An intelligent address recognition algorithm allows DM8606AF to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by DM8606AF to use on Building Internet access to prevent multiple users sharing one port traffic.

1.2 Features

- Supports four 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces and two MII/GPSI ports.
- Supports 2048 MAC addresses table with 4-ways associative hash algorithm.
- Supports four queue for QoS
- Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 256 bytes per block
- Supports Aging function Enable/Disable.
- Supports per port Single/Dual color mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet lengths up to 1522/1522(Default)/1536/1784 bytes in maximum.
- Broadcast/Multicast Storming Filter function.
- Supports 802.1Q VLAN. Up to 16 VLAN groups are implemented by the last four bits of VLAN ID.
- 2bit MAC clone to support multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32-bits smart counter for per port RX/TX byte/packet count, error count and collision count, 16-bits smart counter for per port err count and collision count.
- Supports PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8V/3.3V power supply.
- 1.0W low power consumption.

1.3 Applications

DM8606AF in 128-pin QFP:

- SOHO 5-port switch.
- 5-port switch + Router with MII CPU interface.

1.4 Block Diagram

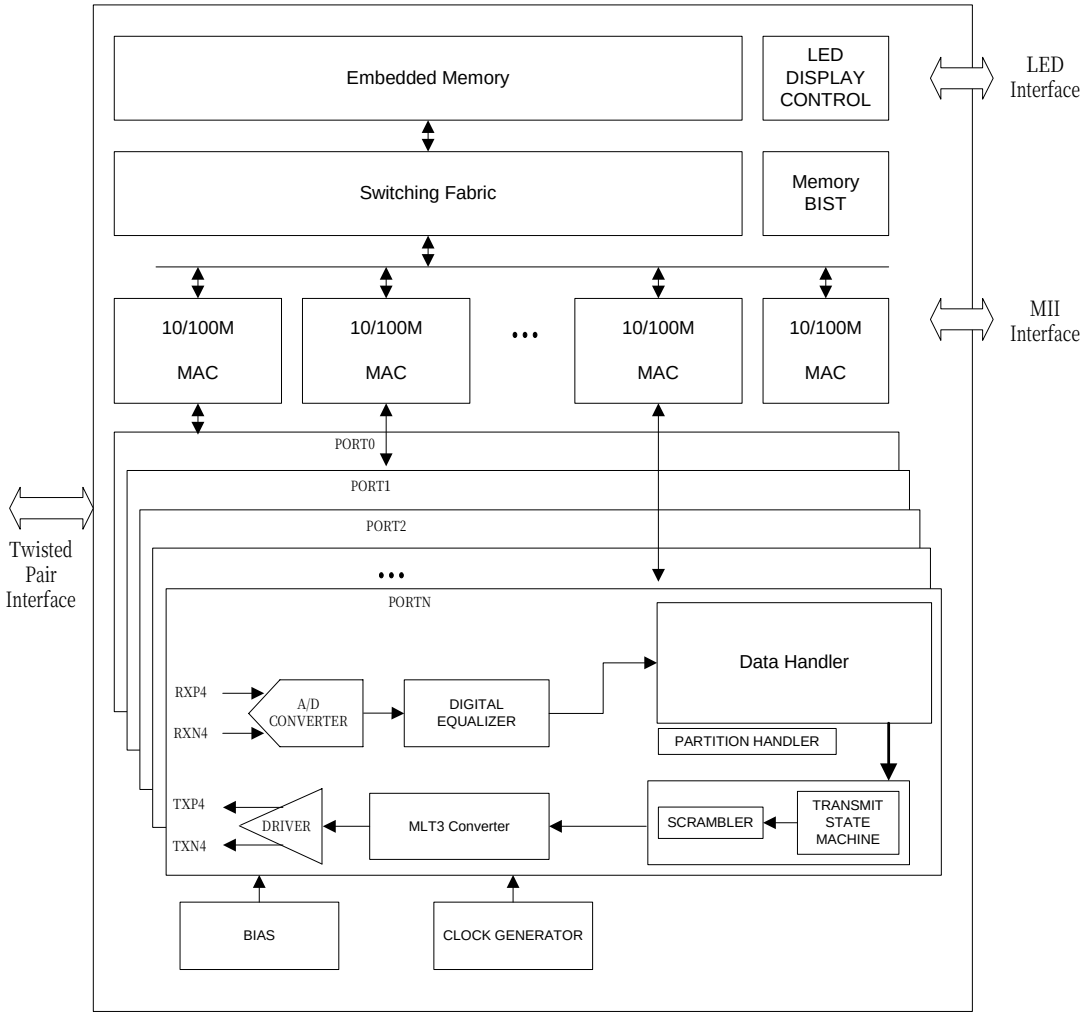


Figure 1-1 DM8606AF Block Diagram

1.5 Abbreviations

BER	Bit Error Rate
CFI	Canonical Format Indicator
COL	Collision
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CS	Chip Select
DA	Destination Address
DI	Data Input
DO	Data Output
EDI	EEPROM Data Input
EDO	EEPROM Data Output

EECS	EEPROM Chip Select
EESK	EEPROM Clock
ESD	End of Stream Delimiter
FEFI	Far End Fault Indication
FET	Field Effect Transistor
FLP	Fast Link Pulse
GND	Ground
GPSI	General Purpose Serial Interface
IPG	Inter-Packet Gap
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller
MDIX	MDI Crossover
MII	Media Independent Interface
NRZI	Non Return to Zero Inverter
NRZ	Non Return to Zero
PCS	Physical Coding Sub-layer
PHY	Physical Layer
PLL	Phase Lock Loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
QoS	Quality of Service
QFP	Quad Flat Package
RST	Reset
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Errors
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
SA	Source Address
SOHO	Small Office Home Office
SSD	Start of Stream Delimiter
SQE	Signal Quality Error
TOS	Type of Service
TP	Twisted Pair
TTL	Transistor Transistor Logic
TXCLK	Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXN	Transmission Negative
TXP	Transmission Positive

1.6 Conventions

1.6.1 Data Lengths

qword	64-bits
dword	32-bits
word	16-bits
byte	8 bits
nibble	4 bits

1.6.2 Pin Types

Pin Type	**Description**
I	Input
O	Output
I/O	Bi-directional
OD	Open drain
SCHE	Schmitt Trigger
PD	internal pull-down
PU	internal pull-up

1.6.2 Register Types

Register Type	**Description**
RO	Read-only
WO	Write-only
RW	Read/Write

Chapter 2 Interface Description

2.1 Pin Diagram

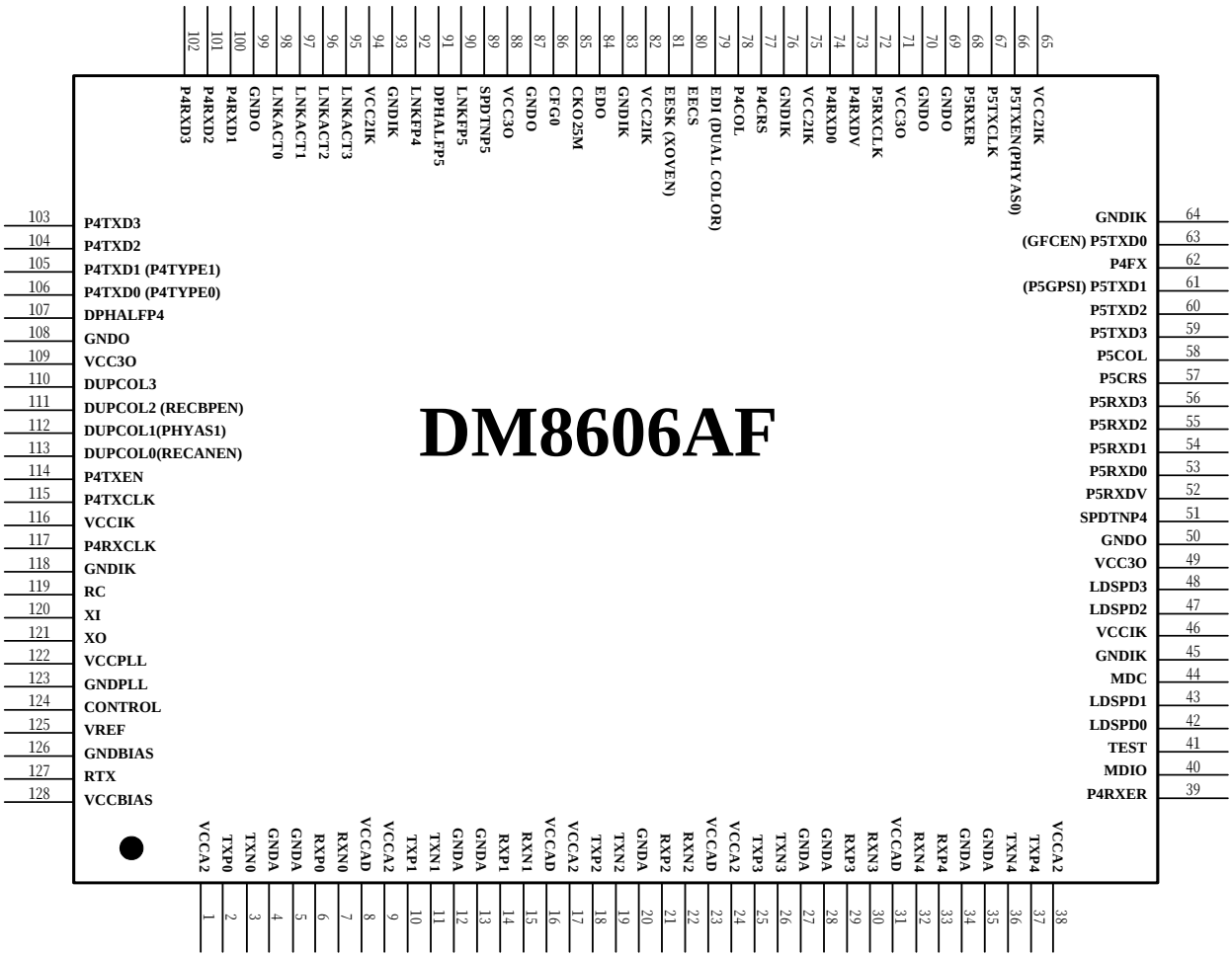


Figure 2-1 4 TP/FX PORT + 2 MII PORT 128 Pin Diagram

2.2 Pin Description by Function

DM8606AF pins are categorized into one of the following groups:

- Section 2.2.1 Twisted Pair Interface
- Section 2.2.2 5th Port (Port4 MII) Interfaces
- Section 2.2.3 6th Port (Port5 MII) Interfaces
- Section 2.2.4 LED Interface
- Section 2.2.5 EEPROM/Management Interface
- Section 2.2.6 Power/Ground, 48 pins
- Section 2.2.7 Miscellaneous

Note:

- "Section 1.6.2 Pin Types" can be used for reference.

2.2.1 Twisted Pair Interface

Pin#	Pin Name	Type	Descriptions
6, 14, 21, 29, 33	RXP[0:4]	I/O, Analog	Twisted Pair Receive Input Positive.
7, 15, 22, 30, 32	RXN[0:4]	I/O, Analog	Twisted Pair Receive Input Negative.
2, 10, 18, 25, 37	TXP[0:4]	I/O, Analog	Twisted Pair Transmit Output Positive.
3, 11, 19, 26, 36	TXN[0:4]	I/O, Analog	Twisted Pair Transmit Output Negative.

2.2.2 5th Port (Port4 MII) Interfaces

Pin#	Pin Name	Type	Descriptions
106	MMII_P4TXD[0]	O, 8mA, PD	Port4 MAC MII Transmit Data Bit 0. The bit[0] of MAC MII Transmit data of port4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD[0]	I, PD	Port4 PCS MII Transmit Data Bit 0. The bit[0] of PCS MII Transmit data of port4. Synchronous to the rising edge of PMII_P4TXCLK.
	Setting P4TYPE0	I, PD	Port4 Bus Type configuration 0. DM8606AF provides 4 bus type for port 4. See CFG0 pin description for more detail. During power on reset, value will be latched by DM8606AF at the rising edge of RESETL(RC) as P4TYPE0.

Pin#	Pin Name	Type	Descriptions
105	MMII_P4TXD[1]	O, 8mA, PD	Port4 MAC MII Transmit Data Bit 1. The bit[1] of MAC MII Transmit data of port4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD[1]	I, PD	Port4 PCS MII Transmit Data Bit 1. The bit[1] of PCS MII Transmit data of port4. Synchronous to the rising edge of PMII_P4TXCLK.
	Setting P4TYPE1	I, PD	Port4 Bus Type configuration 1. See CFG0 pin description for more detail. During power on reset, value will be latched by DM8606AF at the rising edge of RESETL(RC) as P4TYPE1.
104	MMII_P4TXD[2]	O, 8mA, PD	Port4 MAC MII Transmit Data Bit 2. The bit[2] of MAC MII Transmit data of port4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD[2]	I, PD	Port4 PCS MII Transmit Data Bit 2. The bit[2] of PCS MII Transmit data of port4. Synchronous to the rising edge of PMII_P4TXCLK.
103	MMII_P4TXD[3]	O, 8mA, PD	Port4 MAC MII Transmit Data Bit 3. The bit[3] of MAC MII Transmit data of port4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD[3]	I, PD	Port4 PCS MII Transmit Data Bit 3. The bit[3] of PCS MII Transmit data of port4. Synchronous to the rising edge of PMII_P4TXCLK.
62	P4FX	I, PD	Port4 Fiber selection for PCS MII/PHY mode. During power on reset, value will be latched by DM8606AF at the rising edge of RESETL(RC) as P4FX. 0: Port4 as TX port. 1: Port4 as FX port.
114	MMII_P4TXEN	O, 8mA, PD	Port4 MAC MII Transmit Enable.
	PMII_P4TXEN	I, PD	Port4 PCS MII Transmit Enable.
74	MMII_P4RXD[0]	I PD	Port4 MAC MII Receive Data Bit 0. The bit[0] of MAC MII Receive data of port4. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD[0]	O, 8mA, PD	Port4 PCS MII Receive Data Bit 0. The bit[0] of MAC MII Receive data of port4. Synchronous to the rising edge of PMII_P4RXCLK.

Pin#	Pin Name	Type	Descriptions
100	MMII_P4RXD[1]	I PD	Port4 MAC MII Receive Data Bit 1. The bit[1] of MAC MII Receive data of port4. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD[1]	O, 8mA, PD	Port4 PCS MII Receive Data Bit 1. The bit[1] of MAC MII Receive data of port4. Synchronous to the rising edge of PMII_P4RXCLK.
101	MMII_P4RXD[2]	I PD	Port4 MAC MII Receive Data Bit 2. The bit[2] of MAC MII Receive data of port4. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD[2]	O, 8mA, PD	Port4 PCS MII Receive Data Bit 2. The bit[2] of MAC MII Receive data of port4. Synchronous to the rising edge of PMII_P4RXCLK.
102	MMII_P4RXD[3]	I PD	Port4 MAC MII Receive Data Bit 3. The bit[3] of MAC MII Receive data of port4. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD[3]	O, 8mA, PD	Port4 PCS MII Receive Data Bit 3. The bit[3] of MAC MII Receive data of port4. Synchronous to the rising edge of PMII_P4RXCLK.
73	MMII_P4RXDV	I, PD	Port4 MAC MII Receive Data Valid. Active high to indicate that the data on MMII_P4RXD[3:0] is valid, Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXDV	O, 8mA PD	Port4 PCS MII Receive Data Valid. Active high to indicate that the data on PMII_P4RXD[3:0] is valid, Synchronous to the rising edge of MMII_P4RXCLK.
39	MII_P4RXER	I, PD	Port4 MAC MII Receive Error. Active high to indicate that there is symbol error on the MMII_P4RXD[3:0]. Only valid in 100M operation.
78	MMII_P4COL	I, PD	Port4 MAC MII Collision input. Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
	PMII_P4COL	O, 8mA, PD	Port4 PCS MII Collision output. This pin is used to output collision status.
77	MMII_P4CRS	I PD	Port4 MAC MII Port Carrier Sense. In full duplex mode, this pin reflects the receive carrier sense situation on medium only; In half duplex, this pin will be high both in receive and transmit condition.

Pin#	Pin Name	Type	Descriptions
	PMII_P4CRS	O, 8mA, PD	Port4 PCS MII Port Carrier Sense. This pin is used to output Carrier Sense status.
117	MMII_P4RXCLK	I, PD	Port4 MAC MII Receive Clock input. 25MHz free running clock in 100M mode and 2.5MHz free running clock in 10M mode.
	PMII_P4RXCLK	O, 8mA, PD	Port4 PCS MII Receive Clock output 25MHz free running clock in 100M mode and 2.5MHz free running clock in 10M mode.
115	MMII_P4TXCLK	I, PD	Port4 MAC MII Transmit clock input. 25MHz free running clock in 100M mode and 2.5MHz free running clock in 10M mode.
	PMII_P4TXCLK	O, 8mA, PD	Port4 MAC MII Transmit clock output. 25MHz free running clock in 100M mode and 2.5MHz free running clock in 10M mode.
107	DHALFP4	I, PD	Port4 Duplex Status Input. When Port4 operates under MAC MII mode, this pin is used to select the duplex mode of Port4. 0 = Full Duplex 1 = Half Duplex
	DUPCOL4	O, 8mA, PD	Port4 Duplex/Collision LED When Port4 operates under PHY or PCS MII mode, in Full duplex mode, this pin acts as DUPLEX LED for Port4, respectively in half duplex mode, it is collision LED for each port. See Chapter 3.22 LED Display for more details.
92	LNKFP4	I, PD	Port4 Port Link Fail Status Input. When Port4 operates under MAC MII mode, this pin is used as link control of Port4. 0 = Link Up 1 = Link Failed
	LNKACT4	O, 8mA, PD	Port4 LINK/Activity LED. When Port4 operates under PHY or PCS MII mode, this pin is used to indicate the link/activity status of Port4, see Chapter 3.22 LED Display for more details.
51	SPDTNP4	I, PD	Port4 Speed Input. When Port4 operates under MAC MII mode, this pin is used to select the operating speed of Port4. 0 = 100M 1 = 10M

Pin#	Pin Name	Type	Descriptions
	LDSPD4	O, 8mA, PD	Port4 Speed LED When Port4 operates under PHY or PCS MII mode, this pin is used to indicate the speed status of Port4, see Chapter 3.22 LED Display for more details.

2.2.3 6th Port (Port5 MII) Interfaces

Pin#	Pin Name	Type	Descriptions
63	MII_P5TXD[0]	O, 4mA, PU	Port5 MII Transmit Data Bit 0. The bit[0] of MII Transmit data of port5. Synchronous to the rising edge of MII_P5TXCLK.
	RMII_P5TXD[0]	O, 4mA, PU	Port5 RMII Transmit Data Bit 0. The bit[0] of RMII Transmit data of port5. Synchronous to the rising edge of REFCLK_IN.
	GPSI_P5TXD	O, 4mA, PU	Port5 GPSI Transmit Data Bit 0. GPSI Transmit data of port5. Synchronous to the rising edge of GPSI_P5TXCLK.
	Setting GFCEN	I, PU	Global Flow Control Enable. Value on this pin will be latched by DM8606AF at the rising edge of RESETL(RC) as flow control enable. 0 = Flow control capability is depended upon the register setting in corresponding port's Basic Control Register. 1 = All ports flow control capability is enabled.
61	MII_P5TXD[1]	O, 4mA, PD	Port5 MII Transmit Data Bit 1. The bit[1] of MII Transmit data of port5. Synchronous to the rising edge of MII_P5TXCLK.
	RMII_P5TXD[1]	O, 4mA, PD	Port5 RMII Transmit Data Bit 1. The bit[1] of RMII Transmit data of port5. Synchronous to the rising edge of REFCLK_IN.
	Setting P5TYPE0	I, PD	Port5 Bus Type configuration 0. Value on this pin will be latched by DM8606AF at the rising edge of RESETL(RC) as port bus mode selection bit 0. Combined with P5TYPE1, DM8606AF provides 3 bus types for Port5. P5TYPE[1:0]: 00 = MII (default) 01 = GPSI 10 = RMII 11 = Reserved and not allowed

Pin#	Pin Name	Type	Descriptions
59	MII_P5TXD[3]	O, 4mA, PD	Port5 MII Transmit Data Bit 3. The bit[3] of MII Transmit data of port5. Synchronous to the rising edge of MII_P5TXCLK.
	Setting SDIO_MD	I, PD	SDC/SDIO Mode Selection. Value on this pin will be latched by DM8606AF at the rising edge of RESETL(RC) for SDIO 32/16 bits selection. 0 : 32 bits mode. (default) 1 : 16 bits mode. Same timing as MDC/MDIO.
60	MII_P5TXD[2]	O, 4mA PD	Port5 MII Transmit Data Bit 2. The bit[2] of MII Transmit data of port5. Synchronous to the rising edge of MII_P5TXCLK.
	Setting P5TYPE1	I, PD	Port5 Bus Type configuration 1. Value on this pin will be latched by DM8606AF at the rising edge of RESETL(RC) as port bus mode selection bit 1. See P5TYPE0 for more details.
66	MII_P5TXEN	O, 8mA, PD	Port5 MII Transmit Enable. Active high to indicate that the data on MII_P5TXD[3:0] is valid. Synchronous to the rising edge of MII_P5TXCLK.
	RMII_P5TXEN	O, 8mA, PD	Port5 RMII Transmit Enable. Active high to indicate that the data on RMII_P5TXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
	GPSI_P5TXEN	O, 8mA, PD	Port5 GPSI Transmit Enable. Active high to indicate that the data on GPSI_P5TXD is valid. Synchronous to the rising edge of GPSI_P5TXCLK.
	Setting PHYAS0	I, PD	PHY Address Bit 0. During power on reset, value will be latched by DM8606AF at the rising edge of RESETL(RC) as PHY starts address select. PHYAS[1:0]=00 and PHY address start from 01000_B.
53	MII_P5RXD[0]	I, PD	Port5 MII Receive Data Bit 0 The bit[0] of MII Receive data of Port5. Synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5RXD[0]	I, PD	Port5 RMII Receive Data Bit 0 The bit[0] of RMII Receive data of Port5. Synchronous to the rising edge of REFCLK_IN.
	GPSI_P5RXD	I, PD	Port5 GPSI Receive Data. GPSI Receive data of Port5. Synchronous to the rising edge of GPSI_P5RXCLK.

Pin#	Pin Name	Type	Descriptions
54	MII_P5RXD[1]	I, PD	Port5 MII Receive Data Bit 1. The bit[1] of MII Receive data of Port5. Synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5RXD[1]	I, PD	Port5 RMII Receive Data Bit 1. The bit[1] of RMII Receive data of Port5. Synchronous to the rising edge of REFCLK_IN.
55	MII_P5RXD[2]	I, PD	Port5 MII Receive Data Bit 2. The bit[2] of MII Receive data of Port5. Synchronous to the rising edge of MII_P5RXCLK.
56	MII_P5RXD[3]	I, PD	Port5 MII Receive Data Bit 3. The bit[3] of MII Receive data of Port5. Synchronous to the rising edge of MII_P5RXCLK.
52	MII_P5RXDV	I, PD	Port5 MII Receive Data Valid. Active high to indicate that the data on MII_P5RXD[3:0] is valid. Synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5CRSDV	I, PD	Port5 RMII Carrier Sense and Receive Data Valid. Active high to indicate that the data on RMII_P5RXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
68	MII_P5RXER	I, PD	Port5 MII Receive Error. Active high to indicate that there is a symbol error on MII_P5RXD[3:0]. Only valid in 100M operation.
	RMII_P5RXER	I, PD	Port5 RMII Receive Error. Active high to indicate that there is a symbol error on RMII_P5RXD[1:0]. Only valid in 100M operation.
58	MII_P5COL	I, PD	Port5 MII Collision Input. Active high to indicate that there is a collision on the medium. Stay low in full duplex operation.
	GPSI_P5COL	I, PD	Port5 GPSI Collision Input. Active high to indicate that there is a collision on the medium. Stay low in full duplex operation.
57	MII_P5CRS	I, PD	Port5 MII Carrier Sense. In full duplex mode, this pin reflects the receive carrier sense situation on medium only; In half duplex, this pin will be high both in receive and transmit condition.
	GPSI_P5CRS	I, PD	Port5 GPSI Carrier Sense. In full duplex mode, this pin reflects the receive carrier sense situation on medium only; In half duplex, this pin will be high both in receive and transmit condition.

Pin#	Pin Name	Type	Descriptions
72	MII_P5RXCLK	I, PD	Port5 MII Receive Clock Input. It is 25MHz free running clock in 100M mode and 2.5MHz free running clock in 10M mode.
	REFCLK_IN	I, PD	RMII 50MHz Reference Clock Input. This pin is used as 50MHz reference clock signal input pin when Port5 operates in RMII mode.
	GPSI_P5RXCLK	I, PD	Port5 GPSI Receive Clock Input. This pin is non-continuous 10MHz Clock input.
67	MII_P5TXCLK	I, PD	Port5 MII Transmit Clock Input. It is 25MHz free running clock in 100M mode and 2.5MHz free running clock in 10M mode.
	REFCLK_OUT	O, 8mA, PD	RMII 50MHz Reference Clock Output. This pin is used as 50MHz reference clock signal output pin when Port5 operates in RMII mode.
	GPSI_P5TXCLK	I, PD	Port5 GPSI Transmit Clock Input. It is continuous 10MHz clock input.
91	DHALFP5	I, PD	Port5 Duplex Status Input. 0 = Full Duplex 1 = Half Duplex
90	LNKFP5	I, PD	Port5 Link Fail Status Input. 0 = Link Up 1 = Link Failed
89	SPDTNP5	I, PD	Port5 Speed Input. 0 = 100M 1 = 10M

2.2.4 LED Interface

Pin#	Pin Name	Type	Descriptions
95,96, 97,98	LNKACT[3:0]	O, 8mA, PD	LINK/Activity LED[3:0] of Port 3 to 0. Used to indicate corresponding port's link/activity status, see Chapter 3.22 LED Display for more details.
110	DUPCOL[3]	O, 8mA, PD	Duplex/Collision LED[3] of Port3. In full duplex mode, this pin acts as DUPLEX LED for Port3, respectively in half duplex mode, it is collision LED for each port. see Chapter 3.22 LED Display for more details.
111	DUPCOL[2]	O, 8mA, PU	Duplex/Collision LED[2] of Port2. Active low "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication

Pin#	Pin Name	Type	Descriptions
	Setting BPEN	I, PU	Recommend Back-Pressure in Half-Duplex. Value on this pin will be latched by DM8606AF during power on reset as the back-pressure enable in half-duplex mode. 0 = Disable Back-Pressure. 1 = Enable Back-pressure.
112	DUPCOL[1]	O, 8mA, PD	Duplex/Collision LED[1] of Port1. In full duplex mode, this pin acts as Port1 DUPLEX LED; in half duplex mode, it is collision LED for Port1. see Chapter 3.22 LED Display for more details.
	Setting PHYAS1	I, PD	PHY Address Bit 1. Value on this pin will be latched by DM8606AF during power on reset as the PHY address recommend value bit 1. See PHYAS0 description for more details.
113	DUPCOL[0]	O, 8mA, PU	Duplex/Collision LED[0] of Port0. In full duplex mode, this pin acts as Port0 DUPLEX LED; in half duplex mode, it is collision LED for Port0. see Chapter 3.22 LED Display for more details.
	Setting ANEN	I, PU	Auto Negotiation Enable. Only valid for Twisted pair interface. 0 = Disable all TP port auto negotiation capability. 1 = Enable all TP port auto negotiation capability.
48, 47, 43, 42	LDSPD[3:0]	O, 8mA, PD	Speed LED[3:0] of Port 3 to 0. Used to indicate corresponding port's speed status. "0" for 100Mb/s, "1" for 10Mb/s, see Chapter 3.22 LED Display for more details.

2.2.5 EEPROM/Management Interface

Pin#	Pin Name	Type	Descriptions
84	EDO	I, PU	EEPROM Data Output. Serial data input from EEPROM. This pin is internally pull-up. During DM8606AF initialization, DM8606AF will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tri-state during this period.
80	EECS	O, 4mA, PD	EEPROM Chip Select. This pin is active high chip enable for EEPROM. When RESETL is low, it will be Tri-state. Internally Pull-down

Pin#	Pin Name	Type	Descriptions
	IFSEL	I, PD	Interface Selection. After DM8606AF initialization process is done, this pin is used to select using EEPROM interface or SDC/SDIO interface. 0 = SDC/SDIO interface. 1 = EEPROM interface
81	EECK	I/O, 4mA PD	EEPROM Serial Clock. During the DM8606AF initialize itself, this pin is used to output clock to EEPROM. After DM8606AF initialization process is done, this pin is used as EEPROM interface clock input if IFSEL = 1.
	SDC	I, PD	Serial Management interface Clock input. If IFSEL=0, this pin is used as serial management interface clock input.
	Setting XOVEN	I, PD	Cross Over Enable. Value on this pin (active low) will be latched by DM8606AF at the rising edge of RESETL(RC) for Port 4~0 crossover auto detect (Only available in TP interface). 0 = Disable 1 = Enable
79	EDI	I/O, 8mA, PD	EEPROM Serial Data Input. During the DM8606AF initialize itself, this pin is used to output address and command to access EEPROM. After DM8606AF initialization process is done, this pin becomes an input pin to monitor EEPROM data if IFSEL = 1.
	SDIO	I/O, 8mA, PD	Serial Management interface Data Input/Output. If IFSEL=0, this pin is used as data input/output pin of serial management interface.
	Setting LEDMODE	I	Choose LED Display Mode. Value on this pin will be latched by DM8606AF at the rising edge of RESETL(RC) as single/dual color LED mode control signal. see Chapter 3.22 LED Display for more details. 0 = Single color mode for LED. 1 = Dual color mode for LED.

2.2.6 Power/Ground, 48 pins

Pin#	Pin Name	Type	Descriptions
4,5,12, 13, 20, 27, 28, 34, 35	GNDA	I	Ground Used by AD Block.
1, 9, 17, 24, 38	VCCA2	I	1.8V, Power Used by TX Line Driver.
8, 16, 23, 31	VCCAD	I	3.3V, Power Used by AD Block.
126	GNDBIAS	I	Ground Used by Bias Block
128	VCCBIAS	I	3.3V, Power Used by Bias Block.
123	GNDPLL	I	Ground Used by PLL
122	VCCPLL	I	1.8V, Power Used by PLL
45, 64, 76, 83, 93, 118	GNDIK	I	Ground Used by Digital Core
46, 65, 75, 82, 94, 116	VCCIK	I	1.8V, Power Used by Digital Core
50, 69, 70, 87, 99, 108	GNDO	I	Ground Used by Digital Pad
49, 71, 88, 109	VCC3O	I	3.3V, Power Used by Digital Pad.

2.2.7 Miscellaneous

Pin#	Pin Name	Type	Descriptions
85	CKO25M	O, 8mA, PD	25M Clock Output. Free running 25MHz clock output (even during power on reset)
124	CONTROL	I/O, Analog	FET Control Signal. The pin is used to control FET for 3.3V to 1.8V regulator. External 0.1uF capacitor connection to ground for noise filter, even the pin is un-connected.
127	RTX	I, Analog	Constant Voltage Reference TX Resistor. Add 1.1K %1 resister to GND.
125	VREF	I, Analog	Analog Reference Voltage. Used by Internal Bias Circuit for voltage reference. External 0.1uF capacitor connection to ground for noise filter.
119	RC	I, SCHE	RC Input for Power On Reset. This pin is sampled by using the 25MHz free running clock signal which input from XI to generate the low-active reset signal, RESETL.

Pin#	Pin Name	Type	Descriptions
120	XI	I, Analog	25MHz Crystal / Oscillator Input. 25MHz Crystal or Oscillator Input. Variation is limited to +/- 50ppm.
121	XO	O, Analog	25M Crystal Output. When connected to oscillator, this pin should left unconnected.
86	CFG0	I, PU	Configuration 0. Combined with P4TYPE1 and P4TYPE0, DM8606AF provides 3 bus type for port 4. CFG0 P4TYPE[1:0] Description 0 00 PHY Interface 0 01 MAC MII 1 xx PCS MII
40	MDIO	I/O, 8mA, PD	Management Data. MDIO transfers management data in and out of the device synchronous to MDC.
44	MDC	I, SCHE	Management Data Reference Clock. A non-continuous clock input for management usage. DM8606AF will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.
41	TEST	I, PD	TEST Mode. At normal application connect to GND.

Chapter 3 Function Description

3.1 Functional Descriptions

The DM8606AF integrates four 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, four complete 10Base-T modules, 6 port 10/100 switch controller and two 10/100 MII/GPSI MAC and memory into a single chip for both 10Mbits/s, 100Mbits/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbits/s and 100Mbits/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The DM8606AF consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in SSRAM

The interfaces used for communication between PHY block and switch core is MII interface.

Auto MDIX function is supported in this block. This function can be Enable/Disable by hardware pin.

3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)
- The 100Base-X and 10Base-T sections share the following functional blocks.
- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.3 100Base-X Module

The DM8606AF implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in IEEE 802.3. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbits/s PHY loop back is included for diagnostic purpose.

3.4 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s receive data stream. The DM8606AF implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block

3.4.1 A/D Converter

A high performance A/D converter with 125Mhz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; it also possess auto-gain-control capabilities that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.4.2 Adaptive Equalizer and timing Recovery Module

All digital design is especially immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.4.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

3.4.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.4.5 Symbol Alignment

The symbol alignment circuit in the DM8606AF determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.4.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.4.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.4.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.4.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The DM8606AF performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable from the auto negotiation module. When receive, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.4.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.4.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the DM8606AF will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.4.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.5 100Base-TX Transceiver

DM8606AF implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.5.1 Transmit Drivers

The DM8606AF 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.5.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The DM8606AF uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The DM8606AF 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.6.1 Operation Modes

The DM8606AF 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the DM8606AF functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the DM8606AF can simultaneously transmit and receive data.

3.6.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.6.3 Transmit Driver and Receiver

The DM8606AF integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.6.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The DM8606AF implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11h.

3.7 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.8 Jabber Function

The jabber function monitors the DM8606AF output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs.

3.9 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.
The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.10 Automatic Link Polarity Detection

DM8606AF's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses.

3.11 Clock Synthesizer

The DM8606AF implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.12 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The DM8606AF supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority relative to the following list:

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex
- 10Base-T half duplex (lowest priority)

3.13 Memory Block

DM8606AF build in memory is divided as two blocks. One is MAC addressing table and another one is data buffer.

MAC address Learning Table size is 2048 entry with each entry occupy eight bytes length. These eight bytes data include 6 bytes source address, VLAN information, Port information and Aging counter.

Data buffer is divided to 256 bytes/block. DM8606AF buffer management is per port fixed block number and all port share one global buffer. This architecture can get better memory utilization and network balance on different speed and duplex test condition.

Received packet will separate as several 256 bytes/block and chain together. If packet size more than 256 bytes then DM8606AF will chain two or more block to store receiving packet.

3.14 Switch Functional Description

The DM8606AF uses a "store & forward" switching approach for the following reason: Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a "network cache"

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.15 Basic Operation

The DM8606AF receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within same VLAN group, if appropriate. If the destination address is not found in the address table, the DM8606AF treats the packet as a broadcast packet and forwards the packet to the other ports which in same VLAN group.

The DM8606AF automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.15.1 Address Learning

The DM8606AF uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The DM8606AF searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the DM8606AF waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by DM8606AF.

3.15.2 Address Recognition and Packet Forwarding

The DM8606AF forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. Forwarding port must same VLAN with source port.

1) If the DA is an UNICAST address and the address was found in the Address Table, the DM8606AF will check the port number and acts as follows:
   - If the port number is equal to the port on which the packet was received, the packet is discarded.
   - If the port number is different, the packet is forwarded across the bridge.
2) If the DA is an UNICAST address and the address was not found, the DM8606AF treats it as a multicast packet and forwards across the bridge.
3) If the DA is a Multicast address, the packet is forwarded across the bridge.
4) If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by DM8606AF. DM8606AF can issue and learn PAUSE command.
5) DM8606AF will forward the packet with DA of (01-80-C2-00-00-00), filter out the packet with DA of (01-80-C2-00-00-01), and forward the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F)

3.15.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the DM8606AF internally has a 300 seconds timer will aged out (remove) the address from the address table. Aging function can enable/disable by user. Normally, disabling aging function is for security purpose.

3.15.4 Back off Algorithm

The DM8606AF implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. DM8606AF will restart the back off algorithm by choosing 0-9 collision counts. The DM8606AF resets the collision counter after 16 consecutive retransmit trials.

3.15.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits time. The value is 9.6us for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET and 96ns for 1000M. DM8606AF provide option of 92 bit gap in EEPROM to prevent packet lost when turn off Flow Control and clock P.P.M. value difference.

3.15.6 Illegal Frames

The DM8606AF will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will accept by DM8606AF. In case of bypass mode enabled, DM8606AF will support tag and untagged packets with size up to 1522 bytes. In case of non-bypass mode, DM8606AF will support tag packets up to 1526bytes, untagged packets up to 1522bytes.

3.15.7 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the DM8606AF cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An Davicom Semiconductor Inc. proprietary algorithm is implemented inside the DM8606AF to prevent back pressure function cause HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.15.8 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by DM8606AF to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. DM8606AF can issue or receive pause packet.

3.15.9 Old Broadcast Storm filter (0x0b[0]=0 and 0x11[6]=0)

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.0x10[2:0].

Broadcast storm mode after initial:
Time interval : 50ms
The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	7440fps	14880fps	29760fps
Not All 100TX	Disable	744fps	14880fps	2976fps

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	14880fps	29760fps	59520fps
Not All 100TX	Disable	1488ps	2976fps	5952fps

Table 3-1 Old broadcast strom max. packet number

3.15.10 New Broadcast/Multicast Storm filter (0x0b[0]=1 and 0x11[6]=1)

DM8606AF allows users to limit the traffic of the broadcast address (DA=$FFFFFFFFFFF_H$) to prevent them from blocking the switch bandwidth. If users also want to limit the multicast packets (DA[40]=1_B), they can set the Multicast Packet Counted into Storming Counter (see $003B_H$ and $003C_H$) are used to control the broadcast storm.

1. Time Scale. DM8606AF uses 50ms as a scale to meter the storm packets.

Parameter	Rising Threshold	Falling Threshold
All link ports are 100M	100M Threshold (See $003B_H$[12:00])	1/2 100M Threshold
All link ports are not all 100M	10M Threshold (See $003C_H$12:00])	1/2 10M Threshold

Table 3-2 New Broadcast/Multicast Storming Threshold

2. Storm keeps on at least 1.6 seconds if any of the ports meets the rising threshold in the 4 consecutive 50 ms intervals. In these 1.6 seconds, the ports meeting the rising threshold will start to discard the broadcast or multicast packets until the 50 ms interval expires. Users could also disable Input Filter (see $000B_H$[14]) function to forward above packets to the un-congested port instead of discarding directly.

3. Storm finishes. After the 1.6-second storm period, DM8606AF will check the port that makes the storm on. If all of these ports meet the falling threshold in the 2 consecutive 50 ms intervals and no other ports satisfy the rising threshold at the same time, the storm will finish.

3.16 Auto TP MDIX function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connect other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customer can use one by one cable to connect two Switch devices. All these effort need extra cost and not good solution. DM8606AF provide Auto MDIX function which can adjust TX+- and RX+- at correct pin. User can use one by one cable between DM8606AF and other device. This function can be Enable/Disable by hardware pin and EEPROM configuration register 0x01h~0x09h bit 15. If hardware pin set all port at Auto MDIX mode then EEPROM setting is useless. If hardware pin set all port at non Auto MDIX mode then EEPROM can set each port this function enable or disable.

3.17 Port Locking

Port locking function will provide customer simple way to limit per port user number to one. If this function is turn on then DM8606AF will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which not same as locking one will be dropped. DM8606AF provide one MAC address per port. This function is per port setting. When turn on Port Locking function, recommend customer turn off aging function. See EEPROM register 0x12h bit 0~8.

3.18 VLAN setting & Tag/Untag & port-base VLAN

DM8606AF supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by DM8606AF. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13 to register 22) of the configuration content of each port.

DM8606AF also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. DM8606AF learn user define four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first :

* Port VID number at EEPROM register 0x01h~0x09h bit 13~10, register 0x28h~0x2bh and register 0x2ch bit 7~0: DM8606AF will check coming packet. If coming packet is non VLAN packet then DM8606AF will use PVID as VLAN group reference. DM8606AF will use packet's VLAN value when receive tagged packet.

* VLAN Group Mapping Register. EEPROM register 013_H~022_H define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tag port or Untag port by Configuration register Bit 4. The operation of packet between Tag port and Untag port can explain by follow example:

Example1: Port receives Untag packet and send to Untag port.

DM8606AF will check the port user define four bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port then this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

Example2: Port receives Untag packet and send to Tag port.

DM8606AF will check the port user define fours bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

Example3: Port receives Tag packet and send to Untag port.

DM8606AF will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove four bytes with new CRC error. If destination port not same VLAN as receiving port then this packet will be dropped.

Example4: Port receives Tag packet and send to Tag port.

DM8606AF will check the user define packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

3.19 Old Fixed Ingress Bandwidth Control

DM8606AF also supports DM8606F compatible Bandwidth Control with fixed rate. (0x0b[0]=0, see Receive Bandwidth Max [2:0] of 0x31h~0x32h)

000	001	010	011	100	101	110	111
256K	512K	1M	2M	5M	10M	20M	50M

Table 3-3 Fixed Ingress bandwidth control

3.20 New Scalable Egress/Ingress Bandwidth Control

Bandwidth control function is useful on community networks for different levels of service. DM8606AF provides Scalable Egress/Ingress Bandwidth Control. Users can set any value that is based on 64K unit.
(0x0b[0]=1 and 0x33[12]=1, see Receive/Transmit Bandwidth Max [10:0] of 0x31h~0x3ah)

3.21 Priority Setting

It is a trend that data, voice and video will be put on networking, Switch not only deal data packet but also provide service of multimedia data. DM8606AF provides four priority queues on each port and each is assigned a weight. Default rate is 8:4:2:1. User can see Priority Queue Weight Ratio for more detail.

Queue	Weight
Queue 0	Weight = 1
Queue 1	Weight = "Queue 1 Weight" bits in 0025h
Queue 2	Weight = "Queue 1 Weight" bits in 0026h
Queue 3	Weight = "Queue 1 Weight" bits in 0027h

Table 3-4 Priority Queue Weight Ratio

This priority function can set three ways as below:
* By Port Base: Set specific port at specific queue. DM8606AF only check the port priority and not check packet's content VLAN and TOS.
* By VLAN first: DM8606AF check VLAN three priority bit first then IP TOS priority bits.
* By IP TOS first: DM8606AF check IP TOS three priority bit first then VLAN three priority bits.

If port set at VLAN/TOS priority but receiving packet without VLAN or TOS information then port base priority will be used .

3.22 LED Display

Three LED per port are provided by DM8606AF. Link/Act, Duplex/Col & Speed are three LED display of DM8606AF. Dual color LED mode also supported by DM8606AF. For easy production purpose DM8606AF will send test signal to each LED at power on reset stage. EEPROM register $0x12_H$ define LED configuration table.

1. **LED_MODE**: It is the value latched on the EDI pin during the power on reset. It's also used to control the dual or single color mode and is useless when the value wait_init is high.
2. **DUP_COL_SEP** (see 0012_H): Dupcol LEDs indicate the duplex status only.

3. **DHCOL_LED_EN** (see 0030_H): When enabled, pin DUPCOL0 shows col_10m status and pin DUPCOL1 shows col_100m status. These two LEDs are necessary in the dual-speed hub.

DM8606AF LED is active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal add pull high then LED will active Low. If external signal add pull down resister then LED will drive high.

3.22.1 Single Color LED Display

Table 3-5 Single color LED display

Pin Name	Status
LNKACT4/ LNKACT3/ LNKACT2/ LNKACT1/ LNKACT0	These pins have no power-on reset values on them, and DM8606AF uses active low value to drive the led. So the output values of these pins after the power on reset are shown as follows: 1. First period: This period lasts 1.28 sec for LED on test. DM8606AF drives value 0 to open the LED. 2. Second period: This period lasts 0.48 sec for LED off test. DM8606AF drives value 1 to close the LED. 3. Normal Period: This period indicates the link status. 0B, Port links up and LED is ON. 1B, Port links down and LED is OFF. 0/1B, Port links up and is transmitting or receiving. The LED flashes at 10Hz.
LDSPD4/ LDSPD3/ LDSPD2/ LDSPD1/ LDSPD0	The behavior of these pins is the same as the LNKACT, except the normal period. Normal period: This period indicates the speed status. 0B, Port links up and its speed is 100M. LED is ON. 1B, Port links down or its speed is 10M. LED is OFF.
DUPCOL2/ DUPCOL1/ DUPCOL0	These 3 pins have power-on reset values on them. DM8606AF needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows: 1. First period: This period lasts 1.28 sec for LED on test. DM8606AF drives ~value_power_on to open the LED. 2. Second period: This period lasts 0.48 sec for LED off test. DM8606AF drives value_power_on to close the LED. 3. Normal Period: This period indicates the duplex/collision status. ~value_poer_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED flashes at 10Hz.

	0/1B, Port links up and collision is detected. The LED flashes at 10Hz. If DUP_COL_SEP is enabled, the normal period changes its way to display. ~value_poer_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1B, This value is cancelled. LED doesn't blink. If DHCOL_LED_EN is enabled, the display in the normal period is as follows: DUPCOL0: 10m collision indicator. 0/1B, One of the ports links up in 100M half-duplex mode and detects and collision event. The LED flashes at 20Hz. value_power_on = When the above envet is not satisfied, the LED is OFF. DUPCOL1: 100m collision indicator. 0/1B, One of the ports links up in 100M half-duplex mode and detects a collision event. The LED flashes at 20Hz. value_power_on = The above envet is not satisfied, the LED is OFF.
DUPCOL4/ DUPCOL3	The behavior of these pins is the same as the LNKACT, except the normal period. Normal period: This period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED is OFF. 0/1B, Port links up and collision is detected. The LED flashes at 10Hz. If DUP_COL_SEP is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1B, This value is cancelled. LED doesn't blink.

3.22.2 Dual Color LED Display

Users should be careful that DUPCOL LED only supports the single color mode. The only difference between single and dual color for DUPCOL LED is the self-test time.

Table 3-6 Dual color LED display

Pin Name	Status
(LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3)/ (LNKACT2, LDSPD2)/ (LNKACT1, LDSPD1)/ (LNKACT0, LDSPD0)	First Period: Test LED is on with gree color. It lasts 1.28 sec. 01B, LED is on with green color. Second Period: Test LED is on with yellow color. It lasts 1.28 sec. 10B, LED is on with yellow color. Third Period: Test LED off. 00B, LED is off. Normal Period: This period shows the status of the link and speed at the same time. 00B, Port links down. LED is off. 11B, Port links down. LED is off. 01B, Port links up in 100M. LED glows green. 10B, Port links up in 10M. LED glows yellow. 0/1,1B, Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10Hz. 0/1,0B, Pot links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10Hz.
DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1/ DUPCOL0	The behavior of these pins is the same as the single mode, except the self-test period. The LED on test period is 2.56 sec instead of 1.28 sec.

3.22.3 Circuit for Single LED Mode

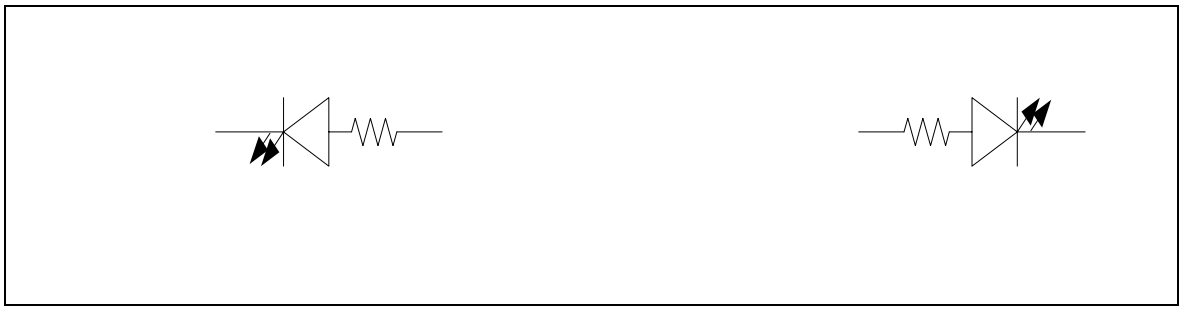


Figure 3-1 Circuit for Single Color LED Mode

3.22.4 Circuit for Dual LED Mode

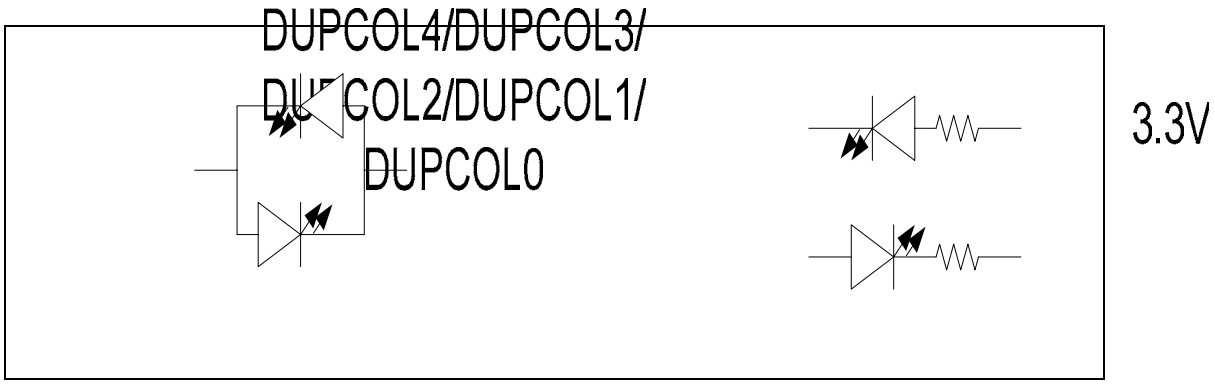


Figure 3-2 Circuit for Dual Color LED Mode

3.23 Port4 and Port5 MII connection

In DM8606AF, there are 3 different configurations (Normal PHY, MAC type MII and PCS type MII, CFG0) for Port4. If Port4 is configured in normal PHY mode, then it is identical to Port0~Port3 and Port4's MII signals are ignored. If Port4 is configured in MAC type MII mode, it can be used for the HomePNA application and embedded single PHY will not be used. In DM8606AF, the most popular is to configure Port4 as the PCS type MII for the router's WAN port application. Users can see **Figure 5** and **Figure 6** for more clear picture. For the Port5, there are three different configurations (MAC type MII mode, GPSI mode and RMII, **P5_BUSMD0**) for connecting to CPU's MII/GPSI or RMII interface.

Here we depicted two general router applications of DM8606AF, one is connected to CPU with single MII and another is connected to CPU with dual MII. In **Figure 5**, we can see either LAN to WAN or WAN to LAN, the packets will go through the same MII port. Because the CPU need to send out the packets with the registered MAC ID to the WAN port, and this MAC ID may also come in from the LAN ports. We know the switch learning scheme can't permit the packets with same MAC ID input from different port. In the DM8606AF design, we use the MAC clone and VLAN group to solve this problem. From **Figure 7**, users can have more details for this implementation.

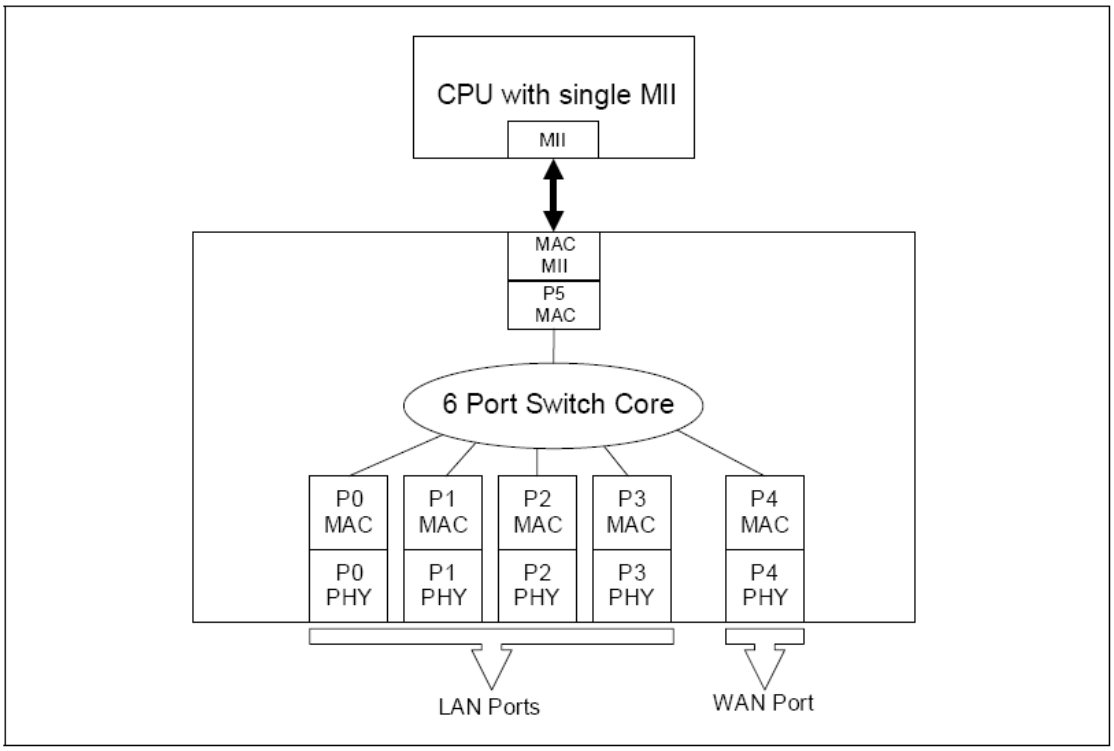


Figure 3-3 DM8606AF to CPU with single MII connection

In **Figure 6**, it shows an easy way to connect the CPU with dual MII for the routing application. In this application, Port4's embedded and isolated PHY will be connected to the WAN port. CPU will act as the bridge to translate the packet's frame for LAN/WAN and use different MII to handle the packets either from LAN to WAN or from WAN to LAN. The isolated PHY is helpful to reduce the BOM cost.

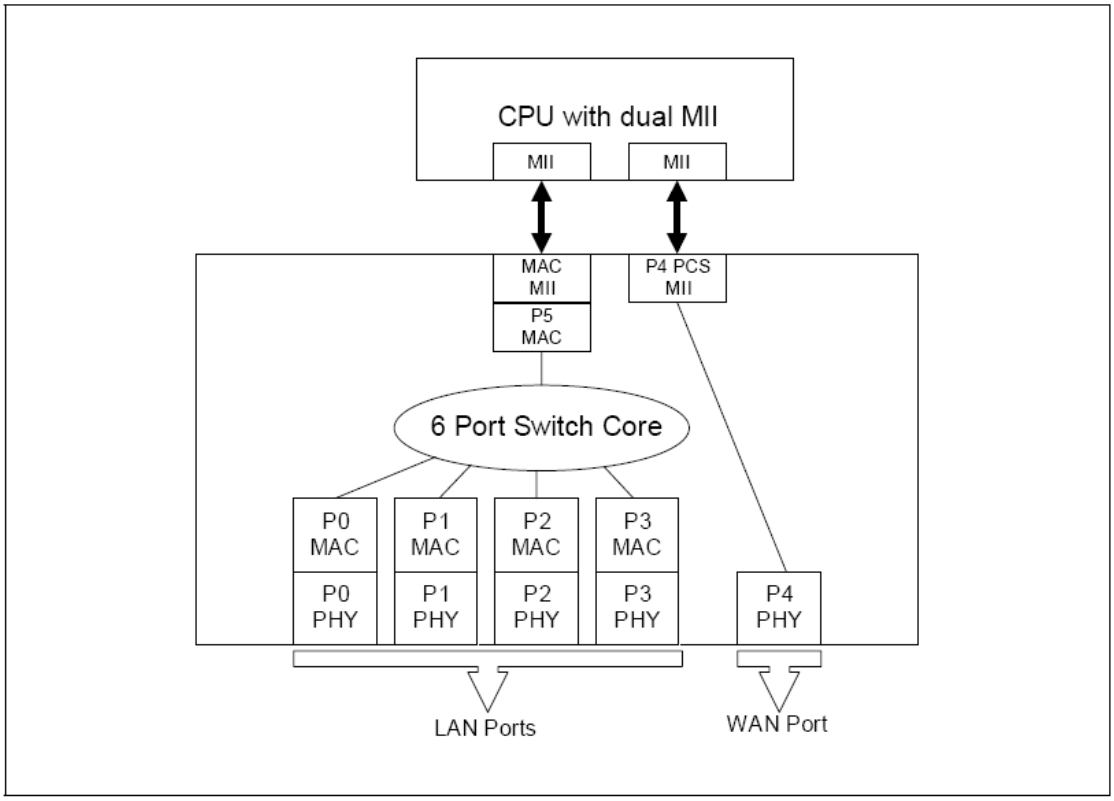


Figure 3-4 DM8606AF to CPU with dual MII connection

Here we use an example to describe how to enable the MAC clone and set the VLAN group to reach this LAN/WAN routing activity.

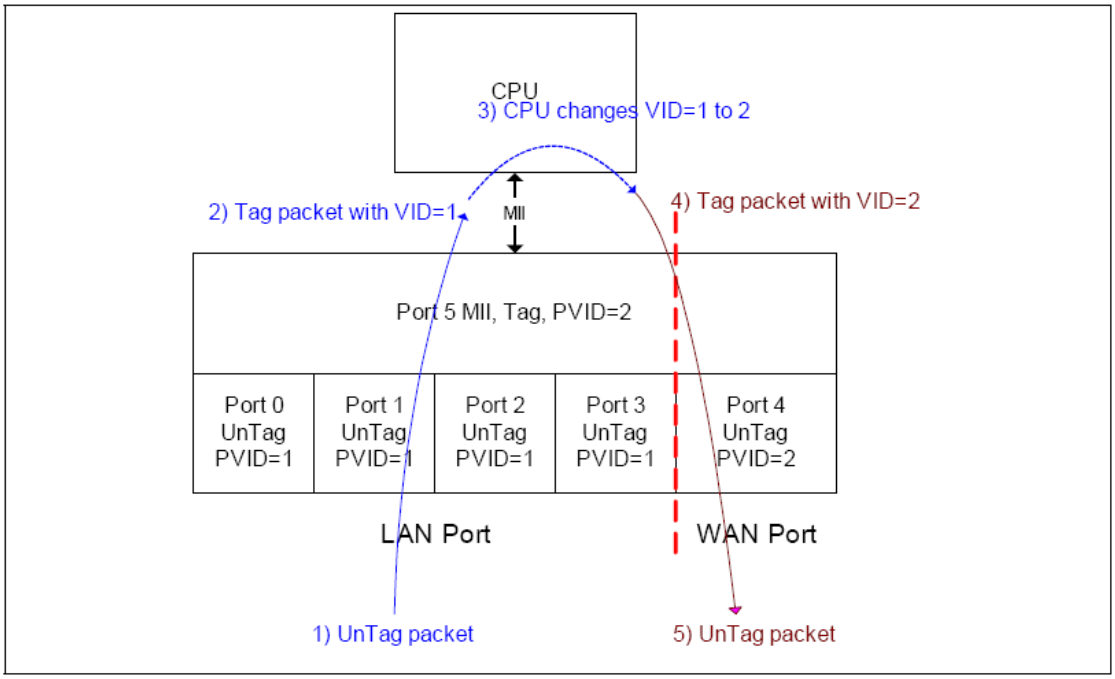


Figure 3-5 MAC Clone Enable and VLAN Setting

Step1: Set DM8606AF to tag-based VLAN mode -- set EEPROM $0x11_H$ to $0xFF20_H$
Step2: Set per port PVID and Tag/UnTag output port --
Port0, UnTag, PVID=1, set EEPROM 0x01 H to 0x840F H
Port1, UnTag, PVID=1, set EEPROM 0x03 H to 0x840F H
Port2, UnTag, PVID=1, set EEPROM 0x05 H to 0x840F H
Port3, UnTag, PVID=1, set EEPROM 0x07 H to 0x840F H
Port4, UnTag, PVID=2, set EEPROM 0x08 H to 0x880F H
Port5, Tag, PVID=2, set EEPROM 0x09 H to 0x881F H
Step3: Set WAN/LAN group
Group1: Port 0/1/2/3/5, set EEPROM 0x14 H to 0x0155 H
Group2: Port 4/5, set EEPROM 0x15 H to 0x0180 H

If Untag packet received from LAN port and forwards to CPU port, DM8606AF will use ingress port PVID as the egress tag VID. CPU can recognize the source group of the packet by VID. If VID=1, it means the packet is received from the LAN port. Otherwise, if VID=2, it means the packet is received from the WAN port. CPU has to change the tag VID to determine the destination group. The tag packet received from CPU port will follow tag-based VLAN to determine the broadcast domain. If the tag packet with VID=1 will follow VLAN group 1 (LAN group) and the tag packet with VID=2 will follow the

VLAN group 2 (WAN group)

Normally, the MAC mode MII should be connected to the PCS mode MII. But in some applications, we need to connect both MAC mode MII to each other as shown in above figures. In **Figure 6**, due to most of CPU's MII are MAC mode, so Port4 is PCS to MAC connection and Port5 is MAC to MAC connection.

Through the hardware setting, it is easy to set DM8606AF Port5 MII be operating in 100M Full duplex mode. And this kind mode (100M Full) is normally the operation mode to be with CPU, the interface connection is described in the following diagram.

(1) CKO25M is the 25M clock driven out by DM8606AF to fit 100M MII operation. This clock output provides 8mA driving capability and it can directly connected to TXCLK/RXCLK.
(2) Due to it is operated in Full duplex mode, so COL is tied to GND.

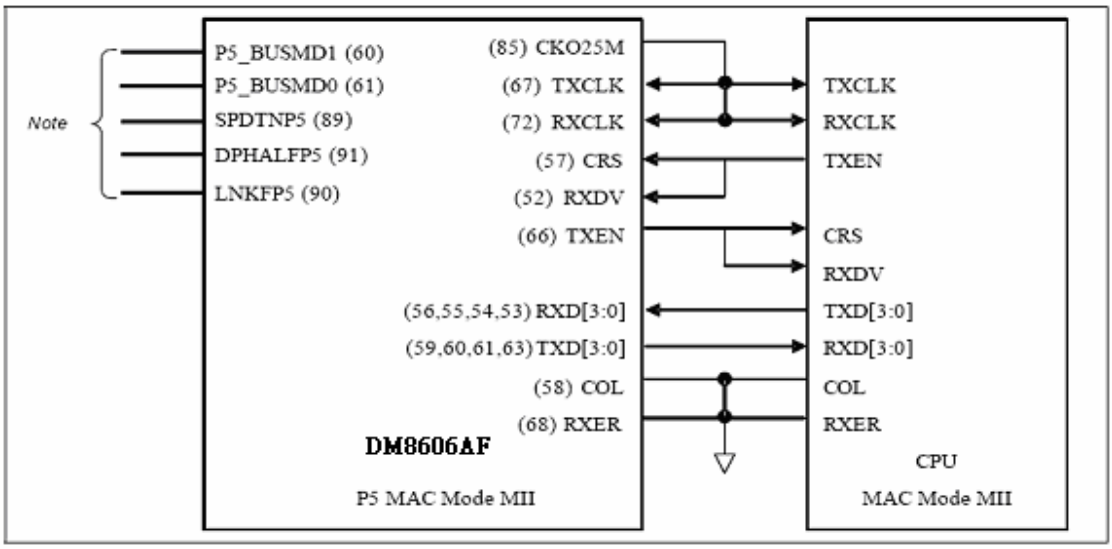


Figure 3-6 100M Full duplex MAC to MAC MII connection

Note:
*1. Pin 60 and pin 61 should be pull low to let P5_BUSMD be latched as "00" and make Port5 be operating in MII mode (**P5_BUSMD0**).*
2. Pin 89 (SPDTNP5) should be pull low or floating to set Port5 be operating in 100Mbit/s.
3. Pin 91 (DPHALFP5) should be pull low or floating to set Port5 be operating in full duplex mode.
4. Pin 90 (LNKFP5) should be pull low or floating to set Port5 Link up.

About the PCS mode MII connect to MAC mode MII, it's very straightforward. If PCS and MAC follow the MII standard timing and users notice the PCB layout balance, it should not be an issue for PCS to connect the MAC. In **Figure 9**, we depicted this interface connection and described how to configure Port4 as the PCS mode MII.

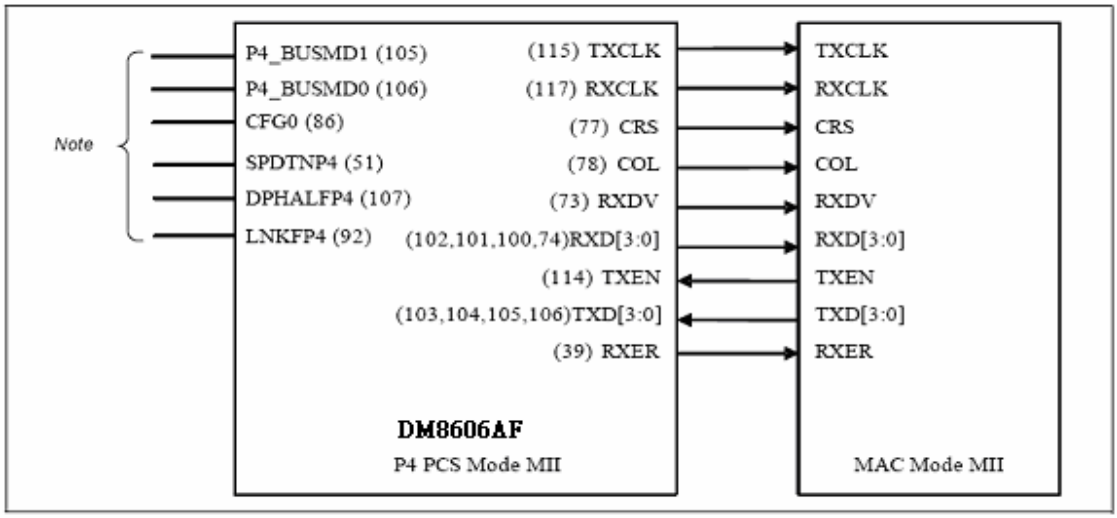


Figure 3-7 PCS to MAC MII connection

Note:
*5. From **CFG0** pin description, we know it needs to set {CFG0, P4_BUSMD[1:0]} as 1xxB to configure Port4 be operating in PCS mode MII. So it doesn't matter the value on P4_BUSMD[1:0] (pin 105 and pin 106) and we only pull high the CFG0 or make it floating (due to it has internally pull high) is ok.*
6. Pin 51 (SPDTNP4) acts as DUPLEX LED for Port 4; in half duplex mode, it is collision LED for each port.
7. Pin 107 (DPHALFP4) used to indicate the speed status of Port 4.
8. Pin 92 (LNKFP4) used to indicate the link/activity status of Port 4.

3.24 EEPROM and SMI interface for Configuration

Three ways are supported to configure the setting in the DM8606AF: (1) Hardware Setting (2) EERPROM Interface (3) SMI Interface. Users could use EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See the following figure as a description.

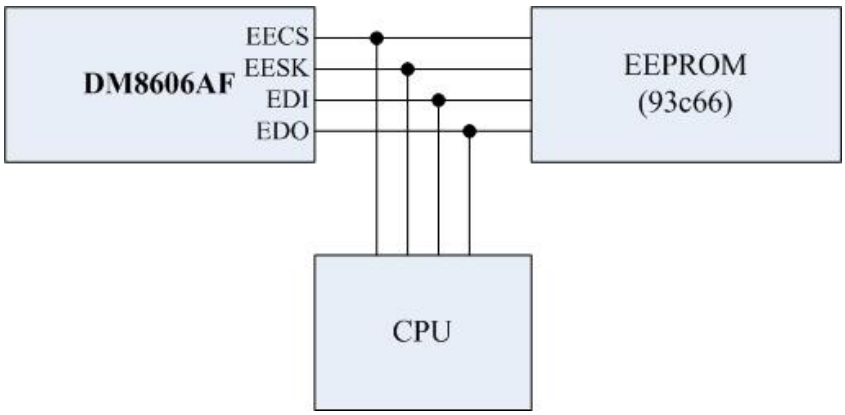


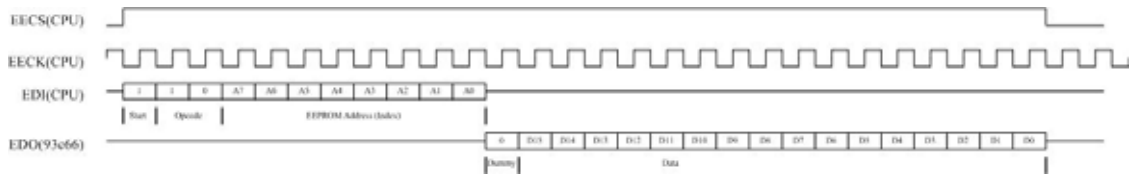
Figure 3-8 Interconnection between DM8606AF, EEPROM and CPU

3.24.1 EEPROM Setting

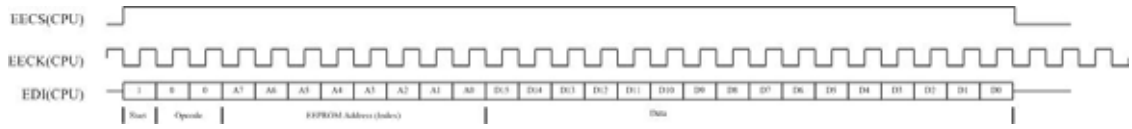
The EEPROM Interface is provided so the users could easily configure the setting without CPU's help. Because the EEPROM Interface is the same as the 93lc66, it also allows the CPU to write the EEPROM register and renew the 93lc66 at the same time. After the power up or reset (default value from the hardware pins fetched in this stage), the DM8606AF will automatically detect the presence of the EEPROM by reading the address 0 in the 96c66. If the value = 16'h4154, it will read all the data in the 93lc66. If not, the DM8606AF will stop loading the 93lc66. The user also could pull down the EDO to force the DM8606AF not to load the 93lc66. The 93lc66 loading time is around 30ms. Then CPU should give the high-z value in the EECS, EECK and EDI pins in this period if we really want to use CPU to read or write the registers in the DM8606AF.

The EEPROM Interface needs only one Write command to complete a writing operation. If updating the 93lc66 at the same time is necessary, three commands Write Enable, Write, and Write Disable are needed to complete this job (See 93lc66 Spec. for a reference). Users should note that the EERPOM interface only allows the CPU to write the EEPROM register in the DM8606AF and doesn't support the READ command. If CPU gives the Read Command, DM8606AF will not respond and 93lc66 will respond with the value. Users should also note that one additional EECK cycle is needed between any continuous commands (Read or Write).

(1) Read 93lc66 via the EEPROM Interface.



(2) Write EEPROM registers in the DM8606AF.



3.24.2 SMI Interface

The SMI consists of two pins, management data clock (EECK) and management data input/output (EDI). The DM8606AF is designed to support an EECK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin may be needed (pulled to low) if EEPROM interface is also used.

The EDI pin requires a 1.5 KΩ pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. DM8606AF requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EECK. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to management register operation. The next field is management register address. It is 10 bits wide and the most significant bit is transferred first.

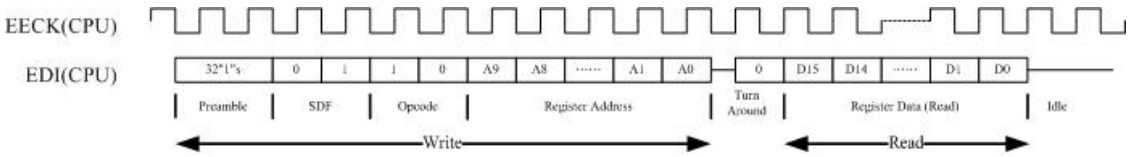
During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the management registers of the DM8606AF.

(1) **Preamble Suppression**
initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI While the DM8606AF will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

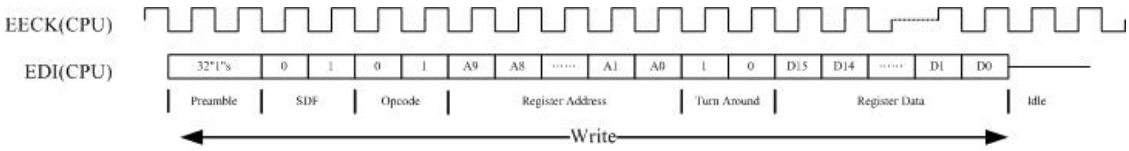
When DM8606AF detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then DM8606AF will tri-

state the EDI pin.

(2) Read Switch Register via SMI Interface



(3) Write Switch Register via SMI Interface



(4) The pin type of EECS, EECK, EDI and EDO during the operation.

Pin Name	Reset Operation	Load EEPROM	Write Operation	Read Operation
EECS	Input	Output	Input	Input
EECK	Input	Output	Input	Input
EDI	Input	Output	Input	Input/Output
EDO	Input	Input	Input	Input

Chapter 4 Register Description

4.1 EEPROM Content

EEPROM provides DM8606AF many options setting such as:

- Port Configuration: Speed, Duplex, Flow Control Capability and Tag/ Untag.
- VLAN & TOS Priority Mapping
- Broadcast Storming rate and Trunk.
- Fiber Select, Auto MDIX select
- VLAN Mapping
- Per Port Buffer number

4.1.1 Memory Map

Register	Definition
0x0000h~0x003fh	EEPROM BAISC Register Map
0x00a0h~0x0143h	Counter and Switch Status Map
0x0200h~0x02ffh	PHY Register Map

4.2 EEPROM Register Map

Register	Bit 15- 8	Bit 7 - 0	Default Value
0x00h	Signature Register		0x4154h
0x01h	Port 0 Basic Control Register		0x040fh
0x02h	Reserved		0x0000h
0x03h	Port 1 Basic Control Register		0x040fh
0x04h	Reserved		0x0000h
0x05h	Port 2 Basic Control Register		0x040fh
0x06h	Reserved		0x0000h
0x07h	Port 3 Basic Control Register		0x040fh
0x08h	Port 4 Basic Control Register		0x040fh
0x09h	Port 5 Basic Control Register		0x040fh
0x0ah	System Control Register 0		0x5802h
0x0bh	System Control Register 1		0x8001h
0x0ch	Reserved		0x0000h
0x0dh	Reserved		0x0000h
0x0eh	VLAN priority Map		0xfa50h
0x0fh	TOS priority Map		0xfa50h
0x10h	System Control Register 2		0x0040h
0x11h	System Control Register 3		0xe300h
0x12h	System Control Register 4		0x3600h

Register	Bit 15- 8	Bit 7 - 0	Default Value
0x13h	Reserved	VLAN Group 0 Port Map	0x01d5h
0x14h	Reserved	VLAN Group 1 Port Map	0x01d5h
0x15h	Reserved	VLAN Group 2 Port Map	0x01d5h
0x16h	Reserved	VLAN Group 3 Port Map	0x01d5h
0x17h	Reserved	VLAN Group 4 Port Map	0x01d5h
0x18h	Reserved	VLAN Group 5 Port Map	0x01d5h
0x19h	Reserved	VLAN Group 6 Port Map	0xffd5h
0x1ah	Reserved	VLAN Group 7 Port Map	0xffd5h
0x1bh	Reserved	VLAN Group 8 Port Map	0xffd5h
0x1ch	Reserved	VLAN Group 9 Port Map	0xffd5h
0x1dh	Reserved	VLAN Group 10 Port Map	0xffd5h
0x1eh	Reserved	VLAN Group 11 Port Map	0x81d5h
0x1fh	Reserved	VLAN Group 12 Port Map	0xffd5h
0x20h	Reserved	VLAN Group 13 Port Map	0xffd5h
0x21h	Reserved	VLAN Group 14 Port Map	0xffd5h
0x22h	Reserved	VLAN Group 15 Port Map	0xffd5h
0x23h	Reserved		0x0000h
0x24h	Reserved		0x0000h
0x25h	Queue 1 Weight		0x2000h
0x26h	Queue 2 Weight		0x4000h
0x27h	Queue 3 Weight		0x8000h
0x28h	Reserved	P0 PVID [11:4]	0x0000h
0x29h	Reserved	P1 PVID [11:4]	0x0000h
0x2ah	Reserved	P2 PVID [11:4]	0x0000h
0x2bh	P4 PVID [11:4]	P3 PVID [11:4]	0x0000h
0x2ch	Address Control / TAG Shift	P5 PVID [11:4]	0xd000h
0x2dh	Reserved		0x4442h
0x2eh	Reserved		0x0000h
0x2fh	PHY Restart Register		0x0000h
0x30h	Miscellaneous Register		0x0987h
0x31h	Basic Bandwidth Control Register		0x0000h
0x32h	Basic Bandwidth Control Register		0x0000h
0x33h	Bandwidth Control Enable Register		0x0000h
0x34h	Expansion Bandwidth Control Register 0		0x0000h
0x35h	Expansion Bandwidth Control Register 1		0x0000h
0x36h	Expansion Bandwidth Control Register 2		0x0000h
0x37h	Expansion Bandwidth Control Register 3		0x0000h
0x38h	Expansion Bandwidth Control Register 4		0x0000h
0x39h	Expansion Bandwidth Control Register 5		0x0000h
0x3ah	Expansion Bandwidth Control Register 6		0x0fc0h
0x3bh	New Strom Register 0		0x0000h
0x3ch	New Strom Register 1		0x0000h

Register	Bit 15- 8	Bit 7 - 0	Default Value
0x3dh	Reserved		0x00ffh
0x3eh	Reserved		0x0000h
0x3fh	Reserved		0x7c80h

4.3 EEPROM Register

4.3.1 Signature Register

offset: 0x00h

Bits	Type	Description	Initial value
15:0	RO	The value must be 4154h(AT)	0x4154h

Note:
DM8606AF will check register 0 value before read all EEPROM content. If this value not match with 0x4154h then other values in EEPROM will be useless. DM8606AF will use internal default value. User cannot write Signature register when programming DM8606AF internal register.

4.3.2 Port0~5 Basic Control Registers

offset: 0x01h, 0x03h, 0x05h, 0x07h, 0x08h, 0x09h

Bits	Type	Description	Initial value
15	R/W	Crossover Auto MDIX enable. 0 = Disable. 1 = Enable. **Note:** Hardware Reset latch value EECK can set global Auto MDIX function. If hardware pin set all port at Auto MDIX then this bit is useless. If hardware pin set chip at non Auto MDIX then this bit can set each port at Auto MDIX.	0x0h
14	R/W	Select FX. 0 = TP mode. 1 = FX mode. ***Note:*** Port4 TX/FX can set by hardware Reset latch value P4FX. If hardware pin set Port4 as FX then this bit is useless. If hardware pin set Port4 as TX then this pin can set Port4 as FX or TX.	0x0h
13:10	R/W	Port VLAN ID, PVID[3:0]. Check Register 0x28h~0x2ch for other PVID[11:4]	0x1h
9:8	R/W	Port-base priority. 00 = Assign packets to Queue 0. 01 = Assign packets to Queue 1. 10 = Assign packets to Queue 2. 11 = Assign packets to Queue 3.	0x0h
7	R/W	Enable port-base priority. 0 = The port priority is disabled. 1 = The port priority is enabled.	0x0h

		Note: If this bit turn on then DM8606AF will not check TOS or VLAN as priority reference. DM8606AF will check port base priority only. DM8606AF default is bypass mode which checks port base priority only. If user wants to check VLAN tag priority then must set chip at Tag mode.	
6	R/W	TOS over VLAN priority. 0 = Use the PRI in the VLAN to assign the priority queue. 1 = Use the PRI in the TOS to assign the priority queue.	0x0h
5	R/W	Port Disable. 0 = Enable port. 1 = Disable port.	0x0h
4	R/W	Output Packet Tagging. 0 = UnTag. 1 = Tag.	0x0h
3	R/W	Duplex. 0 = Half Duplex. 1 = Full Duplex.	0x1h
2	R/W	Speed. 0 = 10M. 1 = 100M.	0x1h
1	R/W	Auto negotiation Enable. 0 = Disable. 1 = Enable.	0x1h
0	R/W	802.3x Flow control command ability. 0 = Disable. 1 = Enable.	0x1h

4.3.3 System Control Register 0

offset: 0x0ah

Bits	Type	Description	Initial value
15:10	RO	Reserved	0x16h
9	R/W	Replaced packet VID 0 by PVID. 1: enable, 0: disable.	0x0h
8	R/W	Replaced packet VID 1 by PVID. 1: enable, 0: disable.	0x0h
7:0	RO	Reserved	0x02h

4.3.4 System Control Register 1

offset: 0x0bh

Bits	Type	Description	Initial value
15	R/W	Disable Far_End_Fault detection. 0 = Enable. 1 = Disable.	0x1h
14:8	RO	Reserved	0x0h

7	R/W	Port3 and Port4 Trunk Enable. 0 = No trunk is enabled 1 = Port3, 4 are trunked.	0x0h
6	R/W	Transmit Short IPG Enable 0 = 96 bits time is used 1 = 88/96 bits time is used	0x0h
5:1	RO	Reserved	0x0h
0	R/W	New EEPROM. 0 = Use Old EEPROM functions. 1 = New EEPROM function is enabled.	0x1h

4.3.5 Reserved Register

offset: 0x0ch~0x0dh

Bits	Type	Description	Initial value
15:0	RO	Reserved	0xfa5h

4.3.6 VLAN Priority Map Register

offset: 0x0eh

Bits	Type	Description	Initial value
15:14	R/W	Mapped priority of tag value = 3'b111.	0x3h
13:12	R/W	Mapped priority of tag value = 3'b110.	0x3h
11:10	R/W	Mapped priority of tag value = 3'b101.	0x2h
9:8	R/W	Mapped priority of tag value = 3'b100.	0x2h
7:6	R/W	Mapped priority of tag value = 3'b011.	0x1h
5:4	R/W	Mapped priority of tag value = 3'b010.	0x1h
3:2	R/W	Mapped priority of tag value = 3'b001.	0x0h
1:0	R/W	Mapped priority of tag value = 3'b000.	0x0h

Note:

Value 3 ~ 0 are for priority queue Q3~Q0 respectively.

The Weight ratio is Q3 : Q2 : Q1: Q0 = 8 : 4 : 2 : 1.

The default is port-base priority for un-tag packet and non-IP frame.

4.3.7 TOS Priority Map Register

offset: 0x0fh

Bits	Type	Description	Initial value
15:14	R/W	Mapped priority of tag value = 3'b111.	0x3h
13:12	R/W	Mapped priority of tag value = 3'b110.	0x3h
11:10	R/W	Mapped priority of tag value = 3'b101.	0x2h
9:8	R/W	Mapped priority of tag value = 3'b100.	0x2h
7:6	R/W	Mapped priority of tag value = 3'b011.	0x1h
5:4	R/W	Mapped priority of tag value = 3'b010.	0x1h
3:2	R/W	Mapped priority of tag value = 3'b001.	0x0h
1:0	R/W	Mapped priority of tag value = 3'b000.	0x0h

Note:
Value 3 ~ 0 are for priority queue Q3~Q0 respectively.
The Weight ratio is Q3 : Q2 : Q1: Q0 = 8 : 4 : 2 : 1.
The default is port-base priority for un-tag packet and non-IP frame.

4.3.8 Normal packet content

Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14~	

4.3.9 VLAN Packet content

DM8606AF will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18~

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The DM8606AF will use bit[3:0] as VLAN group.

4.3.10 TOS IP Packet content

DM8606AF check byte 12 &13 if this value is 0800h then DM8606AF knows this is a TOP priority packet.

Type 0800	IP Header

Byte 12~13 Byte 14~15

IP header define

Byte 14:

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

4.3.11 System Control Register 2

offset: 0x10h

Bits	Type	Description	Initial value
15:8	R/W	Reserved	8'b0
7	R/W	Aging Disable. 0 = Enable aging. 1 = Disable aging.	1'b0
6	RO	Reserved	1'b1
5	R/W	Multicast Packet Counted into the Storm Counter. 0 = Only broadcast packets are counted into the storming counter. 1 = Multicast and broadcast packets are counted into the storming counter.	1'b0
4	R/W	CRC Check Disable. 0 = Enable CRC Check. 1 = Disable CRC check.	1'b0
3	R/W	Back Off Disable. 0 = Back-off is enabled. 1 = Back-off is disabled.	1'b0

Bits	Type	Description	Initial value
2	R/W	Broadcast Storming Enable. It is used in DM8606F style storm control. 0 = Disable. 1 = Enable.	1'b0
1:0	R/W	Broadcast Storming Threshold[1:0]. It is used in DM8606F style storm control. See below table.	2'b0

Note:

Bit[1:0]: Broadcast Storming threshold.

Broadcast storm mode after initial:

- time interval : 50ms

the max. packet number = 7490 in 100Base, 749 in 10Base

Note (Continued):

- per port rising threshold

	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

- per port falling threshold

	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

4.3.12 System Control Register 3

offset: 0x11h

Bits	Type	Description	Initial value
15:13	RO	Reserved	3'b111
12:10	RO	Reserved	3'b0
9:7	R/W	Max Packet Length. 000 = 1518 bytes 001 = 1536 bytes 010 = 1664 bytes 110 = 1522 bytes (default) Other = 1784 bytes	3'b110
6	R/W	New Storming Enable. 0 = Use DM8606F style storming control. 1 = Use DM8606AF style storming control.	1'b0
5	R/W	Tag Base VLAN. 0 = Port VLAN. 1 = Tagged VLAN.	1'b0
4	R/W	MAC Clone Enable 0 = MAC Clone is disabled. Normal mode. Learning with SA only. DM8606AF fill/search MAC table by SA or DA only. 1 = MAC Clone is enabled. MAC Clone mode. Learning with SA, VID0. DM8606AF fill/search MAC table by SA or DA with VID0. This bit can let chip learn two same addresses with different VID0.	1'b0
3	RO	Reserved	1'b0
2	R/W	Interrupt Polarity Inverter. 0 = The interrupt signal is active low. 1 = The interrupt signal is active high.	1'b0
1:0	R/W	Aging Timer Select 00 = 300 sec. 01 = 75 sec. 10 = 18 sec. 11 = 1 sec.	2'b0

Note:

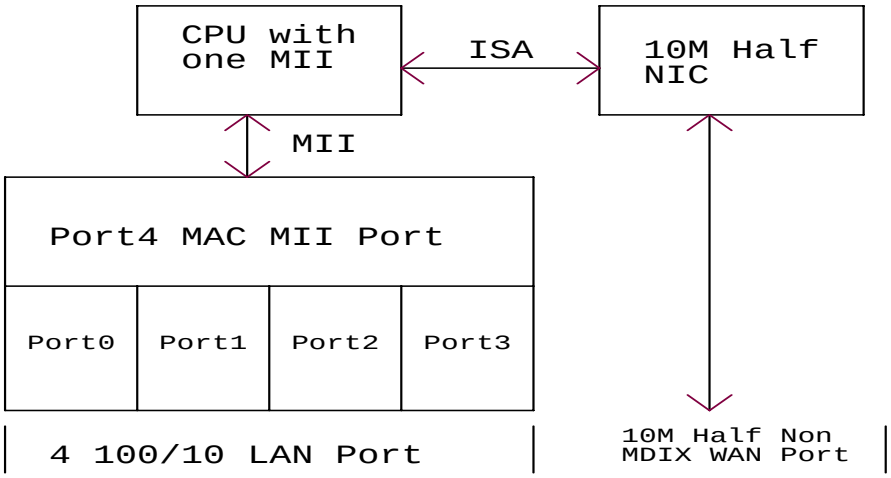
Below is Bit4, 5 VLAN Tag and MAC application example.

Below is some old architecture for a Router. The disadvantages of this are:

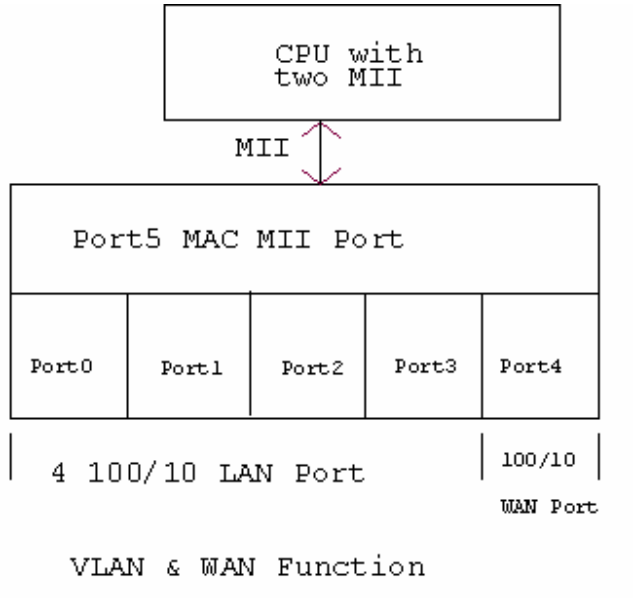
1.WAN ports only support 10M Half-Duplex and non-MDIX function.

2.Need extra 10M NIC i.e. cost.

3.ISA bus will become the bottleneck of the whole system.



Below is the new architecture using the DM8606AF serial chip VLAN function. The advantages of below are:
1. WAN Port can upgrade to 100/10 Full/Half , Auto MDIX.
2. No need for an extra NIC therefore much more economical.
3. High bandwidth of port 5 MII up to 200M speed.



In this application, the CPU's MDC/MDIO interface is used to access all PHY and switch registers in DM8606AF. Port 4 is used as the WAN port and Port 5 is used to connect the CPU. Because the WAN port need to be isolated from the LAN ports due to frames are different and need to be translated by CPU. CPU will act as the bridge to transmit, receive and translate frames between WAN and LAN. This isolated PHY can help to reduce the BOM costs and improve the Gateway router's performance.

New Router application works well on normal application. If user's ISP vendor(cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition happen is there exist two same MAC ID on this Switch. One is original Card and another one is CPU. This will make Switch learning table trouble.
DM8606AF provide MAC Clone function that allow two same MAC address with different VLAN ID0 on learning table. This will solve Lock registration Card's ID issue.

How to Set DM8606AF on Router.

Port0~3: LAN Port.
Port4: WAN Port.
Port5: MII Port as CPU Port.

Step1: Set Register 0x11h bit4 and bit5 to 1.
{Coding: Write Register 0x11h as 0xff30h}
Step2: Set Port0~3 as Untag Port and set PVID=1.
{Coding: Write Register 0x01h, 0x03h, 0x05h, 0x07h as 0x840f. Port0~3 as Untag, PVID=1, Enable MDIX}
Step3: Set Port4 as Untag Port and set PVID=2.
{ Coding:Write Register 0x08h as 0x880fh. Port4 as Untag, PVID=2, Enable MDIX.}
Step4: Set Port5 MII Port as Tag Port and set PVID=2.
{Coding:Write Register 0x09h as 0x881fh. Port5 MII port as Tag, PVID=2.}
Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.
{Coding: Write Register 0x14h as 0x0155h. VLAN1 cover Port0, 1, 2, 3, 5.}
Step6: Group Port4, 5 as VLAN 2.
{Coding: Write Register 0x15h as 0x0180h. VLAN2 cover Port4, 5.}

How MAC Clone Operation:

sure enable. 1/enable, 0/disable.
1. LAN to LAN/CPU Traffic.
DM8606AF LAN traffic to LAN/CPU only. Traffic to another LAN port will be untag packet. Traffic to CPU is Tag packet with VID=1. CPU can check VID to distinguish LAN traffic or WAN traffic.

2. WAN to CPU Traffic.
DM8606AF WAN traffic to CPU only. Traffic to CPU is Tag packet with VID=2. CPU can check VID to distinguish LAN traffic or WAN traffic.

3. CPU to LAN Packet.
DM8606AF CPU Packet to LAN port must add VID=1 in VLAN field. DM8606AF check VID to distinguish LAN traffic or WAN traffic. LAN output packet is Untag.

4. CPU to WAN Packet.
DM8606AF CPU Packet to WAN port must add VID=2 in VLAN filed. DM8606AF check VID to distinguish LAN traffic or WAN traffic. WAN output packet is Untag.

5. DM8606AF learning sequence
DM8606AF will check VLAN mapping setting first then check learning table. User does not worry LAN/WAN traffic mix up.

4.3.13 System Control Register 4

offset: 0x12h

Bits	Type	Description	Initial value
15	R/W	Drop packet when excessive collision happen enable. 1 = Enable, 0 = Disable.	1'b0
14	R/W	Reserved	1'b0
13:12	R/W	Power Saving Select	2'b11
11	R/W	Reserved	1'b0
10:9	R/W	Reserved	2'b11
8	R/W	Port5 MAC Lock. 1: Lock first MAC source address, 0: disable.	1'b0
7	R/W	Port4 MAC Lock. 1: Lock first MAC source address, 0: disable.	1'b0
6	R/W	Port3 MAC Lock. 1: Lock first MAC source address, 0: disable.	1'b0
5	R/W	Reserved	1'b0
4	R/W	Port2 MAC Lock. 1: Lock first MAC source address, 0: disable.	1'b0
3	R/W	Reserved	1'b0
2	R/W	Port1 MAC Lock. 1: Lock first MAC source address, 0: disable.	1'b0
1	R/W	Reserved	1'b0
0	R/W	Port0 MAC Lock. 1: Lock first MAC source address, 0: disable.	1'b0

4.3.14 VLAN Mapping Table Registers

offset: 0x22h ~ 0x13h

Bits	Type	Description	Initial value
15:9	RO	Reserved	0x7fh
8:0	R/W	VLAN mapping table.	0x1d5h

Note:

16 VLAN Group: See Register 0x2ch bit 11=0

Bit0: Port0 Bit2: Port1 Bit4: Port2

Bit6: Port3 Bit7: Port4 Bit8: Port5.

Select the VLAN group ports is to set the corresponding bits to 1.

4.3.15 Reserved Register

offset: 0x24h ~ 0x23h

Bits	Type	Description	Initial value
15:0	R/W	Reserved	0x0h

4.3.16 Port0 PVID bit 11 ~ 4 Configuration Register

offset: 0x28h

Bits	Type	Description	Initial value
15:8	RO	Reserved	8'b0
7:0	R/W	P0VID[11:4], Port0 PVID bit 11~4. These 8 bits combine with register 0x01h Bit [13~10] as full 12 bit VID.	8'b0

4.3.17 Port1 PVID bit 11 ~ 4 Configuration Register

offset: 0x29h

Bits	Type	Description	Initial value
15:8	RO	Reserved	8'b0
7:0	R/W	P1VID[11:4], Port1 PVID bit 11~4. These 8 bits combine with register 0x03h Bit[13~10] as full 12 bit VID.	8'b0

4.3.18 Port2 PVID bit 11~4 Configuration Register

offset: 0x2ah

Bits	Type	Description	Initial value
15:8	RO	Reserved	8'b0
7:0	R/W	P2VID[11:4], Port2 PVID bit 11~4. These 8 bits combine with register 0x05h Bit[13~10] as full 12 bit VID.	8'b0

4.3.19 Port3, 4 PVID bit 11~4 Configuration Register

offset: 0x2bh

Bits	Type	Description	Initial value
15:8	RO	P4VID[11:4], Port4 PVID bit 11~4. These 8 bits combine with register 0x08h Bit[13~10] as full 12 bit VID.	8'b0
7:0	R/W	P3VID[11:4], Port3 PVID bit 11~4. These 8 bits combine with register 0x07h Bit[13~10] as full 12 bit VID.	8'b0

4.3.20 Port5 PVID bit 11~4 & VLAN group shift bits Configuration Register

offset: 0x2ch

Bits	Type	Description	Initial value
15	R/W	Control reserved MAC (0180C2000010-0180C20000FF) 1: Forward, 0: Discard.	1'b1
14	R/W	Control reserved MAC (0180C2000002- 0180C200000F) 1: Forward, 0: Discard.	1'b1
13	R/W	Control reserved MAC (0180C2000001) 1: Forward, 0: Discard.	1'b0
12	R/W	Control reserved MAC (0180C2000000) 1: Forward, 0: Discard.	1'b1
11	R/W	Reserved	0x0h
10:8	R/W	Tag shift for VLAN grouping. Default 3'b000. 3'b000: VID[3:0] 3'b001: VID[4:1] 3'b010: VID[5:2] 3'b011: VID[6:3] 3'b100: VID[7:4] 3'b101: VID[8:5] 3'b110: VID[9:6] 3'b111: VID[10:7]	3'b0
7:0	R/W	P5VID[11:4], Port5 PVID bit 11~4. These 8 bits combine with register 0x09h Bit[13~10] as full 12 bit VID.	8'b0

Note:
Bit[10:8]: VLAN Tag shift register. DM8606AF will select 4 bit from total 12 bit VID as VLAN group reference.
Bit[15:12]: IEEE 802.3 reserved DA forward or drop police.

4.3.21 Reserved Register

offset: 0x2dh

Bits	Type	Description	Initial value
15:0	R/W	Reserved	0x4442h

4.3.22 Reserved Register

offset: 0x2eh

Bits	Type	Description	Initial value
15:0	R/W	Reserved	0x0h

4.3.23 PHY Restart Register

offset: 0x2fh

Bits	Type	Description	Initial value
15:0	R/W	PHY Restart. DM8606AF writes this register to restart all the PHYs in the switch. The value is not important.	0x0h

4.3.24 Miscellaneous Configuration Register

offset: 0x30h

Bits	Type	Description	Initial value
15:13	R/W	Reserved	3'b000
12	R/W	Port 4 LED Mode. 1:Link/Act/Speed 0:LinkAct/DupCol/Speed	1'b0
11	R/W	Reserved	1'b1
10	R/W	Reserved	1'b0
9	R/W	Dual Speed Hub COL_LED Enable. 1: Dual Speed Hub LED display. Port0 Col LED: 10M Col LED. Port1 Col LED: 100M Col LED. 0: Normal LED display.	1'b0
8	R/W	Reserved	1'b1
7	R/W	Reserved	1'b1
6	R/W	MII Speed Double. 1: Port 5 MII RXCLK, TXCLK maximum speed is 50MHz 0: Port 5 MII RXCLK, TXCLK maximum speed is 25MHz	1'b0
5	R/W	MAC Clone Enable Bit[1].	1'b0
4:3	R/W	Reserved	1'b0
2	R/W	Reserved	1'b1
1	R/W	Reserved	1'b1
0	R/W	Reserved	1'b1

4.3.25 Bandwidth Control Register0~3

offset: 0x31h

Bits	Type	Description	Initial value
15	R/W	Port 3 Receive Bandwidth Maximum[3] (r3bw_th1).	1'b0
14:12	R/W	Port 3 Receive Bandwidth Maximum[2:0] (r3bw_th0).	3'b000
11	R/W	Port 2 Receive Bandwidth Maximum[3] (r2bw_th1).	1'b0
10:8	R/W	Port 2 Receive Bandwidth Maximum[2:0] (r2bw_th0).	3'b000

Bits	Type	Description	Initial value
7	R/W	Port 1 Receive Bandwidth Maximum[3] (r1bw_th1).	1'b0
6:4	R/W	Port 1 Receive Bandwidth Maximum[2:0] (r1bw_th0).	3'b000
3	R/W	Port 0 Receive Bandwidth Maximum[3] (r0bw_th1).	1'b0
2:0	R/W	Port 0 Receive Bandwidth Maximum[2:0] (r0bw_th0).	3'b000

4.3.26 Bandwidth Control Register 4~5

offset: 0x32h

Bits	Type	Description	Initial value
15	R/W	Port 1 Transmit Bandwidth Maximum[3] (t1bw_th1).	1'b0
14:12	R/W	Port 1 Transmit Bandwidth Maximum[2:0] (t1bw_th0).	3'b000
11	R/W	Port 0 Transmit Bandwidth Maximum[3] (t0bw_th1).	1'b0
10:8	R/W	Port 0 Transmit Bandwidth Maximum[2:0] (t0bw_th0).	3'b000
7	R/W	Port 5 Receive Bandwidth Maximum[3] (r5bw_th1).	1'b0
6:4	R/W	Port 5 Receive Bandwidth Maximum[2:0] (r5bw_th0).	3'b000
3	R/W	Port 4 Receive Bandwidth Maximum[3] (r4bw_th1).	1'b0
2:0	R/W	Port 4 Receive Bandwidth Maximum[2:0] (r4bw_th0).	3'b000

4.3.27 Bandwidth Control Enable Register

offset: 0x33h

Bits	Type	Description	Initial value
15:13	RO	Reserved	0x0h
12	R/W	DM8606AF New Bandwidth Control Enable. 0 = Disable. 1 = Enable.	1'b0
11	R/W	Port5 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t5bw_th3, t5bw_th2, t5bw_th1, t5bw_th0, 6'b0}Kbps, K=1000.	1'b0
10	R/W	Port4 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t4bw_th3, t4bw_th2, t4bw_th1, t4bw_th0, 6'b0}Kbps, K=1000.	1'b0
9	R/W	Port3 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t3bw_th3, t3bw_th2, t3bw_th1, t3bw_th0, 6'b0}Kbps, K=1000.	1'b0
8	R/W	Port5 Receive Bandwidth Control Enable. 0 = Disable.	1'b0

Bits	Type	Description	Initial value
		1 = Enable. The received bandwidth is {r5bw_th3, r5bw_th2, r5bw_th1, r5bw_th0, 6'b0}Kbps, K=1000.	
7	R/W	Port4 Receive Bandwidth Control Enable 0 = Disable. 1 = Enable. The received bandwidth is {r4bw_th3, r4bw_th2, r4bw_th1, r4bw_th0, 6'b0}Kbps, K=1000.	1'b0
6	R/W	Port3 Receive Bandwidth Control Enable 0 = Disable. 1 = Enable. The received bandwidth is {r3bw_th3, r3bw_th2, r3bw_th1, r3bw_th0, 6'b0}Kbps, K=1000.	1'b0
5	R/W	Port2 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t2bw_th3, t2bw_th2, t2bw_th1, t2bw_th0, 6'b0}Kbps, K=1000.	1'b0
4	R/W	Port2 Receive Bandwidth Control Enable 0 = Disable. 1 = Enable. The received bandwidth is {r2bw_th3, r2bw_th2, r2bw_th1, r2bw_th0, 6'b0}Kbps, K=1000.	1'b0
3	R/W	Port1 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t1bw_th3, t1bw_th2, t1bw_th1, t1bw_th0, 6'b0}Kbps, K=1000.	1'b0
2	R/W	Port1 Receive Bandwidth Control Enable 0 = Disable. 1 = Enable. The received bandwidth is {r1bw_th3, r1bw_th2, r1bw_th1, r1bw_th0, 6'b0}Kbps, K=1000.	1'b0
1	R/W	Port0 Transmit Bandwidth Control Enable. 0 = Disable. 1 = Enable. The transmit bandwidth is {t0bw_th3, t0bw_th2, t0bw_th1, t0bw_th0, 6'b0}Kbps, K=1000.	1'b0
0	R/W	Port0 Receive Bandwidth Control Enable 0 = Disable. 1 = Enable. The received bandwidth is {r0bw_th3, r0bw_th2, r0bw_th1, r0bw_th0, 6'b0}Kbps, K=1000.	1'b0

4.3.28 Extended Bandwidth Control Register 0

offset: 0x34h

Bits	Type	Description	Initial value
15	R/W	Port 5 Transmit Bandwidth Maximum[3] (t5bw_th1).	1'b0
14:12	R/W	Port 5 Transmit Bandwidth Maximum[2:0] (t5bw_th0).	3'b000
11	R/W	Port 4 Transmit Bandwidth Maximum[3] (t4bw_th1).	1'b0

Bits	Type	Description	Initial value
10:8	R/W	Port 4 Transmit Bandwidth Maximum[2:0] (t4bw_th0).	3'b000
7	R/W	Port 3 Transmit Bandwidth Maximum[3] (t3bw_th1).	1'b0
6:4	R/W	Port 3 Transmit Bandwidth Maximum[2:0] (t3bw_th2).	3'b000
3	R/W	Port 2 Transmit Bandwidth Maximum[3] (t2bw_th1).	1'b0
2:0	R/W	Port 2 Transmit Bandwidth Maximum[2:0] (t2bw_th0).	3'b000

4.3.29 Extended Bandwidth Control Register 1

offset: 0x35h

Bits	Type	Description	Initial value
15:12	R/W	Port 3 Receive Bandwidth Maximum[7:4] (r3bw_th2).	4'b0000
11:8	R/W	Port 2 Receive Bandwidth Maximum[7:4] (r2bw_th2).	4'b0000
7:4	R/W	Port 1 Receive Bandwidth Maximum[7:4] (r1bw_th2).	4'b0000
3:0	R/W	Port 0 Receive Bandwidth Maximum[7:4] (r0bw_th2).	4'b0000

4.3.30 Extended Bandwidth Control Register 2

offset: 0x36h

Bits	Type	Description	Initial value
15:12	R/W	Port 1 Transmit Bandwidth Maximum[7:4] (t1bw_th2).	4'b0000
11:8	R/W	Port 0 Transmit Bandwidth Maximum[7:4] (t0bw_th2).	4'b0000
7:4	R/W	Port 5 Receive Bandwidth Maximum[7:4] (r5bw_th2).	4'b0000
3:0	R/W	Port 4 Receive Bandwidth Maximum[7:4] (r4bw_th2).	4'b0000

4.3.31 Extended Bandwidth Control Register 3

offset: 0x37h

Bits	Type	Description	Initial value
15:12	R/W	Port 5 Transmit Bandwidth Maximum[7:4] (t5bw_th2).	4'b0000
11:8	R/W	Port 4 Transmit Bandwidth Maximum[7:4] (t4bw_th2).	4'b0000
7:4	R/W	Port 3 Transmit Bandwidth Maximum[7:4] (t3bw_th2).	4'b0000
3:0	R/W	Port 2 Transmit Bandwidth Maximum[7:4] (t2bw_th2).	4'b0000

4.3.32 Extended Bandwidth Control Register 4

offset: 0x38h

Bits	Type	Description	Initial value
15	R/W	Reserved	1'b0
14:12	R/W	Port 4 Receive Bandwidth Maximum[10:8] (r4bw_th3).	3'b000
11:9	R/W	Port 3 Receive Bandwidth Maximum[10:8] (r3bw_th3).	3'b000
8:6	R/W	Port 2 Receive Bandwidth Maximum[10:8] (r2bw_th3).	3'b000
5:3	R/W	Port 1 Receive Bandwidth Maximum[10:8] (r1bw_th3).	3'b000

Bits	Type	Description	Initial value
2:0	R/W	Port 0 Receive Bandwidth Maximum[10:8] (r0bw_th3).	3'b000

4.3.33 Extended Bandwidth Control Register 5

offset: 0x39h

Bits	Type	Description	Initial value
15	R/W	Reserved	1'b0
14:12	R/W	Port 3 Transmit Bandwidth Maximum[10:8] (r3bw_th3).	3'b000
11:9	R/W	Port 2 Transmit Bandwidth Maximum[10:8] (r2bw_th3).	3'b000
8:6	R/W	Port 1 Transmit Bandwidth Maximum[10:8] (r1bw_th3).	3'b000
5:3	R/W	Port 0 Transmit Bandwidth Maximum[10:8] (t0bw_th3).	3'b000
2:0	R/W	Port 5 Receive Bandwidth Maximum[10:8] (r5bw_th3).	3'b000

4.3.34 Extended Bandwidth Control Register 6

offset: 0x3ah

Bits	Type	Description	Initial value
15:6	R/W	Reserved	0x0h
5:3	R/W	Port 5 Transmit Bandwidth Maximum[10:8] (t5bw_th3).	3'b000
2:0	R/W	Port 4 Transmit Bandwidth Maximum[10:8] (t4bw_th3).	3'b000

4.3.35 New Storm Register 0

offset: 0x3bh

Bits	Type	Description	Initial value
15	R/W	Reserved	1'b0
14	R/W	Storm Drop Enable. 0 = Do not drop in the storming period. 1 = Drop in the storming period.	1'b0
13	R/W	Storm Enable. 0 = Disable DM8606AF style broadcast storm protection. 1 = Enable DM8606AF style broadcast storm protection.	1'b0
12:0	R/W	100M Threshold. It is used when all ports link up in the 100M. The upper bound is reached when the number of the packets received during the 50ms is over 100M Threshold.	13'b0

4.3.36 New Storm Register 1

offset: 0x3ch

Bits	Type	Description	Initial value
15:13	R/W	Reserved	0x0h
12:0	R/W	10M Threshold. See Table 31 for more detail information. It is used when one of ports link up in the 10M. The upper bound is reached when the number of the packets received during the 50ms is over 10M Theshold.	13'b0

4.3.37 Reserved Register

offset: 0x3dh

Bits	Type	Description	Initial value
15:0	R/W	Reserved	0x00ffh

4.3.38 Reserved Register

offset: 0x3eh

Bits	Type	Description	Initial value
15:0	R/W	Reserved	0x0000h

4.3.39 Reserved Register

offset: 0x3fh

Bits	Type	Description	Initial value
15:0	R/W	Reserved	0x7c80h

4.5 Serial Register Map

Register	Bit 15-0	Type	Register	Bit 15-0	Type
0xa0h	Chip Identifier 0	RO	0xa1h	Chip Identifier 1	RO
0xa2h	Port Status 0	RO	0xa3h	Port Status 1	RO
0xa4h	Port Status 2	RO	0xa5h	Reserved	RO
0xa6h	Reserved	RO	0xa7h	Reserved	RO
0xa8h	Port 0 Receive Packet Count Low	RW	0xa9h	Port 0 Receive Packet Count High	RW
0xaah	Reserved	RO	0xabh	Reserved	RO
0xach	Port 1 Receive Packet Count Low	RW	0xadh	Port 1 Receive Packet Count High	RW
0xaeh	Reserved	RO	0xafh	Reserved	RO
0xb0h	Port 2 Receive Packet Count Low	RW	0xb1h	Port 2 Receive Packet Count High	RW
0xb2h	Reserved	RO	0xb3h	Reserved	RO
0xb4h	Port 3 Receive Packet Count Low	RW	0xb5h	Port 3 Receive Packet Count High	RW
0xb6h	Port 4 Receive Packet Count Low	RW	0xb7h	Port 4 Receive Packet Count High	RW
0xb8h	Port 5 Receive Packet Count Low	RW	0xb9h	Port 5 Receive Packet Count High	RW
0xbah	Port 0 Receive Packet Byte Count Low	RW	0xbbh	Port 0 Receive Packet Byte Count High	RW
0xbch	Reserved	RO	0xbdh	Reserved	RO
0xbeh	Port 1 Receive Packet Byte Count Low	RW	0xbfh	Port 1 Receive Packet Byte Count High	RW
0xc0h	Reserved	RO	0xc1h	Reserved	RO
0xc2h	Port 0 Receive Packet Byte Count Low	RW	0xc3h	Port 0 Receive Packet Byte Count High	RW
0xc4h	Reserved	RO	0xc5h	Reserved	RO
0xc6h	Port 3 Receive Packet Byte Count Low	RW	0xc7h	Port 3 Receive Packet Byte Count High	RW
0xc8h	Port 4 Receive Packet Byte Count Low	RW	0xc9h	Port 4 Receive Packet Byte Count High	RW
0xcah	Port 5 Receive Packet Byte Count Low	RW	0xcbh	Port 5 Receive Packet Byte Count High	RW
0xcch	Port 0 Transmit Packet Count Low	RW	0xcdh	Port 0 Transmit Packet Count High	RW
0xceh	Reserved	RO	0xcfh	Reserved	RO
0xd0h	Port 1 Transmit Packet Count Low	RW	0xd1h	Port 1 Transmit Packet Count High	RW
0xd2h	Reserved	RO	0xd3h	Reserved	RO
0xd4h	Port 2 Transmit Packet Count Low	RW	0xd5h	Port 2 Transmit Packet Count High	RW
0xd6h	Reserved	RO	0xd7h	Reserved	RO
0xd8h	Port 3 Transmit Packet Count Low	RW	0xd9h	Port 3 Transmit Packet Count High	RW
0xdah	Port 4 Transmit Packet Count Low	RW	0xdbh	Port 4 Transmit Packet Count High	RW
0xdch	Port 5 Transmit Packet Count Low	RW	0xddh	Port 5 Transmit Packet Count High	RW
0xdeh	Port 0 Transmit Packet Byte Count Low	RW	0xdfh	Port 0 Transmit Packet Byte Count High	RW
0xe0h	Reserved	RO	0xe1h	Reserved	RO
0xe2h	Port 1 Transmit Packet Byte Count Low	RW	0xe3h	Port 1 Transmit Packet Byte Count High	RW
0xe4h	Reserved	RO	0xe5h	Reserved	RO
0xe6h	Port 2 Transmit Packet Byte Count Low	RW	0xe7h	Port 2 Transmit Packet Byte Count High	RW
0xe8h	Reserved	RO	0xe9h	Reserved	RO
0xeah	Port 3 Transmit Packet Byte Count Low	RW	0xebh	Port 3 Transmit Packet Byte Count High	RW
0xech	Port 4 Transmit Packet Byte Count Low	RW	0xedh	Port 4 Transmit Packet Byte Count High	RW
0xeeh	Port 5 Transmit Packet Byte Count Low	RW	0xefh	Port 5 Transmit Packet Byte Count High	RW
0xf0h	Port 0 Collision Count Low	RW	0xf1h	Port 0 Collision Count High	RW
0xf2h	Reserved	RO	0xf3h	Reserved	RO

Register	Bit 15-0	Type	Register	Bit 15-0	Type
0xf4h	Port 1 Collision Count Low	RW	0xf5h	Port 1 Collision Count High	RW
0xf6h	Reserved	RO	0xf7h	Reserved	RO
0xf8h	Port 2 Collision Count Low	RW	0xf9h	Port 2 Collision Count High	RW
0xfah	Reserved	RO	0xfbh	Reserved	RO
0xfch	Port 3 Collision Count Low	RW	0xfdh	Port 3 Collision Count High	RW
0xfeh	Port 4 Collision Count Low	RW	0xffh	Port 4 Collision Count High	RW
0x100h	Port 5 Collision Count Low	RW	0x101h	Port 5 Collision Count High	RW
0x102h	Port 0 Error Count Low	RW	0x103h	Port 0 Error Count High	RW
0x104h	Reserved	RO	0x105h	Reserved	RO
0x106h	Port 1 Error Count Low	RW	0x107h	Port 1 Error Count High	RW
0x108h	Reserved	RO	0x109h	Reserved	RO
0x10ah	Port 2 Error Count Low	RW	0x10bh	Port 2 Error Count High	RW
0x10ch	Reserved	RO	0x10dh	Reserved	RO
0x10eh	Port 3 Error Count Low	RW	0x10fh	Port 3 Error Count High	RW
0x110h	Port 4 Error Count Low	RW	0x111h	Port 4 Error Count High	RW
0x112h	Port 5 Error Count Low	RW	0x113h	Port 5 Error Count High	RW
0x114h	Over Flow Flag 0 Low	RC	0x115h	Over Flow Flag 0 High	RC
0x116h	Over Flow Flag 1 Low	RC	0x117h	Over Flow Flag 1 High	RC
0x118h	Over Flow Flag 2 Low	RC	0x119h	Over Flow Flag 2 High	RC
0x11ah ~ 0x13fh	Reserved	RO			
0x140h	Counter Control Low	RW	0x141h	Counter Control High	RW
0x142h	Control Status Low	RO	0x143h	Control Status High	RO

4.6 Serial Register Description

4.6.1 Chip Identifier 0 Register

offset: 0xa0h

Bits	Type	Description	Initial value
15:4	RO	Product Code[11:0]	0x102h
3:0	RO	Version number	0x2h

4.6.2 Chip Identifier 1 Register

offset: 0xa1h

Bits	Type	Description	Initial value
15:4	RO	Reserve	0x0h
3:0	RO	Product Code[15:12]	0x7h

4.6.3 Port Status 0 Register

offset: 0xa2h

Bits	Type	Description	Initial value
15:12	RO	Reserved	0x0h
11	RO	Port 1 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable	0x0h
10	RO	Port 1 Duplex Status 1: Full Duplex. 0: Half Duplex.	0x0h
9	RO	Port 1 Speed Status: 1: 100Mb/s 0: 10 Mb/s	0x0h
8	RO	Port 1 Linkup Status: 1: Link is established. 0: Link is not established.	0x0h
7:4	RO	Reserved	0x0h
3	RO	Port 0 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable	0x0h
2	RO	Port 0 Duplex Status 1: Full Duplex. 0: Half Duplex.	0x0h
1	RO	Port 0 Speed Status: 1: 100Mb/s 0: 10 Mb/s	0x0h

Bits	Type	Description	Initial value
0	RO	Port 0 Linkup Status: 1: Link is established. 0: Link is not established.	0x0h

4.6.4 Port Status 1 Register

offset: 0xa3h

Bits	Type	Description	Initial value
15	RO	Port 4 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable	0x0h
14	RO	Port 4 Duplex Status 1: Full Duplex. 0: Half Duplex.	0x0h
13	RO	Port 4 Speed Status: 1: 100Mb/s 0: 10 Mb/s	0x0h
12	RO	Port 4 Linkup Status: 1: Link is established. 0: Link is not established.	0x0h
11	RO	Port 3 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable	0x0h
10	RO	Port 3 Duplex Status 1: Full Duplex. 0: Half Duplex.	0x0h
9	RO	Port 3 Speed Status: 1: 100Mb/s 0: 10 Mb/s	0x0h
8	RO	Port 3 Linkup Status: 1: Link is established. 0: Link is not established.	0x0h
7:4	RO	Reserved	0x0h
3	RO	Port 2 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable	0x0h
2	RO	Port 2 Duplex Status 1: Full Duplex. 0: Half Duplex.	0x0h
1	RO	Port 2 Speed Status: 1: 100Mb/s 0: 10 Mb/s	0x0h
0	RO	Port 2 Linkup Status:	0x0h

Bits	Type	Description	Initial value
		1: Link is established. 0: Link is not established.	

4.6.5 Port Status 2 Register

offset: 0xa4h

Bits	Type	Description	Initial value
15:5	RO	Reserved	0x0h
4	RO	Port 5 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable	0x0h
3	RO	Port 5 Duplex Status 1: Full Duplex. 0: Half Duplex.	0x0h
2	RO	Reserved	0x0h
1	RO	Port 5 Speed Status. 1 = 100Mb/s. 0 = 10Mb/s.	0x0h
0	RO	Port 5 Linkup Status: 1: Link is established. 0: Link is not established.	0x0h

4.6.6 Reserved Register

offset: 0xa5h ~ 0xa7h

Bits	Type	Description	Initial value
15:0	RO	Reserved	0x0h

4.6.7 Counter Low Register

offset: 0xa8h ~ 0x113h

Bits	Type	Description	Initial value
15:0	RO	Counter[15:0]	0x0h

4.6.8 Counter High Register

offset: 0xa8h ~ 0x113h

Bits	Type	Description	Initial value
15:0	RO	Counter[31:16]	0x0h

4.6.9 Over Flow Flag 0 Register

offset: 0x114h

Bits	Type	Description	Initial value
15	RC	Overflow of Port 3 Receive Packet Byte Count	0x0h
14	RO	Reserved	0x0h
13	RC	Overflow of Port 2 Receive Packet Byte Count	0x0h
12	RO	Reserved	0x0h
11	RC	Overflow of Port 1 Receive Packet Byte Count	0x0h
10	RO	Reserved	0x0h
9	RC	Overflow of Port 0 Receive Packet Byte Count	0x0h
8	RC	Overflow of Port 5 Receive Packet Count	0x0h
7	RC	Overflow of Port 4 Receive Packet Count	0x0h
6	RC	Overflow of Port 3 Receive Packet Count	0x0h
5	RO	Reserved	0x0h
4	RC	Overflow of Port 2 Receive Packet Count	0x0h
3	RO	Reserved	0x0h
2	RC	Overflow of Port 1 Receive Packet Count	0x0h
1	RO	Reserved	0x0h
0	RC	Overflow of Port 0 Receive Packet Count	0x0h

4.6.10 Over Flow Flag 1 Register

offset: 0x115h

Bits	Type	Description	Initial value
15:12	RO	Reserved	0x0h
1	RC	Overflow of Port 5 Receive Packet Byte Count	0x0h
0	RC	Overflow of Port 4 Receive Packet Byte Count	0x0h

4.6.11 Over Flow Flag 2 Register

offset: 0x116h

Bits	Type	Description	Initial value
15	RO	Overflow of Port 3 Transmit Packet Byte Count	0x0h
14	RO	Reserved	0x0h
13	RO	Overflow of Port 2 Transmit Packet Byte Count	0x0h
12	RO	Reserved	0x0h
11	RO	Overflow of Port 1 Transmit Packet Byte Count	0x0h
10	RO	Reserved	0x0h
9	RO	Overflow of Port 0 Transmit Packet Byte Count	0x0h
8	RO	Overflow of Port 5 Transmit Packet Count	0x0h
7	RO	Overflow of Port 4 Transmit Packet Count	0x0h
6	RO	Overflow of Port 3 Transmit Packet Count	0x0h

Bits	Type	Description	Initial value
5	RO	Reserved	0x0h
4	RO	Overflow of Port 2 Transmit Packet Count	0x0h
3	RO	Reserved	0x0h
2	RO	Overflow of Port 1 Transmit Packet Count	0x0h
1	RO	Reserved	0x0h
0	RO	Overflow of Port 0 Transmit Packet Count	0x0h

4.6.12 Over Flow Flag 3 Register

offset: 0x117h

Bits	Type	Description	Initial value
15:2	RO	Reserved	0x0h
1	RC	Overflow of Port 5 Transmit Packet Byte Count	0x0h
0	RC	Overflow of Port 4 Transmit Packet Byte Count	0x0h

4.6.13 Over Flow Flag 4 Register

offset: 0x118h

Bits	Type	Description	Initial value
15	RC	Overflow of Port 3 Error Count	0x0h
14	RO	Reserved	0x0h
13	RC	Overflow of Port 2 Error Count	0x0h
12	RO	Reserved	0x0h
11	RC	Overflow of Port 1 Error Count	0x0h
10	RO	Reserved	0x0h
9	RC	Overflow of Port 0 Error Count	0x0h
8	RC	Overflow of Port 5 Collision Count	0x0h
7	RC	Overflow of Port 4 Collision Count	0x0h
6	RC	Overflow of Port 3 Collision Count	0x0h
5	RO	Reserved	0x0h
4	RC	Overflow of Port 2 Collision Count	0x0h
3	RO	Reserved	0x0h
2	RC	Overflow of Port 1 Collision Count	0x0h
1	RO	Reserved	0x0h
0	RC	Overflow of Port 0 Collision Count	0x0h

4.6.14 Over Flow Flag 5 Register

offset: 0x119h

Bits	Type	Description	Initial value
15:2	RO	Reserved	0x0h
1	RC	Overflow of Port 5 Error Count	0x0h

Bits	Type	Description	Initial value
0	RC	Overflow of Port 4 Error Count	0x0h

4.6.15 Counter Control Low Register

offset: 0x140h

Bits	Type	Description	Initial value
15:8	RO	Reserved	0x0h
7	RW	Busy/Access Start. 1 = The counter control is busy, or users should write 1'b1 into this bit to start the access when the engine is free. 0 = The counter control is free.	0x0h
6	RW	0 = Indirect Read Counter 1 = Renew Port Counter	0x0h
5:0	RW	Indirect Read Counter: It means the counter address. Renew Port Counter: It means the counters on each port to renew.	0x0h

4.6.16 Counter Control High Register

offset: 0x141h

Bits	Type	Description	Initial value
15:0	RO	Reserved	0x0h

4.6.17 Counter Status Low Register

offset: 0x142h

Bits	Type	Description	Initial value
15:0	RO	Counter[15:0]	0x0h

4.6.18 Counter Status High Register

offset: 0x143h

Bits	Type	Description	Initial value
15:0	RO	Counter[31:16]	0x0h

4.8 PHY Register Description

4.8.1 Control Register of Port0~4

ffset: 0x200, 0x220, 0x240, 0x260, 0x280

Bits	Type	Name	Description	Initial value
15	R/W, SC	RST	RESET 1 – PHY Reset 0 – Normal operation Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values The software reset process takes 25us to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.	0x0h
14	R/W	LPBK	Loop Back Enable 1 – Enable loopback mode 0 – Disable Loopback mode This bit controls the PHY loopback operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register	0x0h
13	R/W	SPEED_LSB	Speed Selection LSB 0.6, 0.13 0 0 10 Mbits/s 0 1 100 Mbits/s 1 0 Reserved 1 1 Reserved Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). If it is fiber mode, 0.13 is always 1. Any write to this bit will have no effect.	0x1h
12	R/W	ANEN	Auto Negotiation Enable 1 – Enable auto negotiation process 0 – Disable Auto negotiation process This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the PI_RECANEN pin detects a logic 1 input level in Twisted-Pair Mode. If it is set when fiber mode is configured, any write to this bit	0x1h

Bits	Type	Name	Description	Initial value
			will be ignored.	
11	R/W	PDN	Power Down Enable 1 – Power Down 0 – Normal Operation Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY into power down mode. During the power down mode, TXP/TXN and all LED outputs are tri-stated and the MII interfaces are isolated.	0x0h
10	R/W	ISO	Isolate PHY from Network 1 – Isolate PHY from MII 0 – Normal Operation Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the PHY does not respond to TXD, TXEN and TXER inputs, and it presents a high impedence on its TXC, RXC, CRSDV, RXER, RXD, COL and CRS outputs.	0x0h
9	R/W, SC	ANEN_RST	Restart Auto Negotiation 1 – Restart Auto Negotiation Process 0 – Normal Operation Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced.	0x0h
8	R/W	DPLX	Duplex Mode 1 – Full Duplex mode 0 – Half Duplex mode If auto negotiation is disabled, this bit determines the duplex mode for the link.	0x1h
7	R/W	COLTST	Collision Test 1 – Enable COL signal test 0 – Disable COL signal test When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN.	0x0h
6	RO	SPEED_MSB	Speed Selection MSB Set to 0 all the time indicate that the PHY does not support 1000 Mbits/s function.	0x0h
5:0	RO	Reserved	Not Applicable	0x00h

4.8.2 Status Register of Port0~4

offset: 0x201, 0x221, 0x241, 0x261, 0x281

Bits	Type	Name	Description	Initial value
15	RO	CAP_T4	100Base-T4 Capable Set to 0 all the time to indicate that the PHY does not support 100Base-T4	0x0h
14	RO	CAP_TXF	100Base-X Full Duplex Capable Set to 1 all the time to indicate that the PHY does support Full Duplex mode	0x1h
13	RO	CAP_TXH	100Base-X Half Duplex Capable Set to 1 all the time to indicate that the PHY does support Half Duplex mode	0x1h
12	RO	CAP_TF	10M Full Duplex Capable TP : Set to 1 all the time to indicate that the PHY does support 10M Full Duplex mode FX : Set to 0 all the time to indicate that the PHY does not support 10M Full Duplex mode	0x1h 0x0h
11	RO	CAP_TH	10M Half Duplex Capable TP : Set to 1 all the time to indicate that the PHY does support 10M Half Duplex mode FX : Set to 0 all the time to indicate that the PHY does not support 10M Half Duplex mode	0x1h 0x0h
10	RO	CAP_T2	100Base-T2 Capable Set to 0 all the time to indicate that the PHY does not support 100Base-T2	0x0h
9:7	RO	Reserved	Not Applicable	0x0h
6	RO	CAP_SUPR	MF Preamble Suppression Capable This bit is hardwired to 1 indicating that the PHY accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification.	0x1h
5	RO	AN_COMP	Auto Negotiation Complete 1 – Auto Negotiation process completed 0 – Auto Negotiation process not completed If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected.	0x0h
4	RO	REM_FLT	Remote Fault Detect 1 – Remote Fault detected 0 – Remote Fault not detected This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05h) is set or the receive channel meets the far end fault indication	0x0h

Bits	Type	Name	Description	Initial value
			function criteria. It is unlatched when this register is read.	
3	RO	CAP_ANEG	Auto Negotiation Ability 1 – Capable of auto negotiation 0 – Not capable of auto negotiation TP : This bit is set to 1 all the time, indicating that PHY is capable of auto negotiation. FX : This bit is set to 0 all the time, indicating that PHY is not capable of auto negotiation in Fiber Mode.	0x1h 0x0h
2	RO	LINK	Link Status 1 – Link is up 0 – Link is down This bit reflects the current state of the link –test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status	0x0h
1	RO	JAB	Jabber Detect 1 – Jabber condition detected 0 – Jabber condition not detected	0x0h
0	RO	EXTREG	Extended Capability 1 – Extended register set 0 – No extended register set This bit defaults to 1, indicating that the PHY implements extended registers.	0x0h

4.8.3 PHY Identifier Register of Port0~4

offset: 0x202, 0x222, 0x242, 0x262, 0x282

Bits	Type	Name	Description	Initial value
15:0	RO	PHY-ID[15:0]	IEEE Address	0x002Eh

4.8.4 PHY Identifier Register of Port0~4

offset: 0x203, 0x223, 0x243, 0x263, 0x283

Bits	Type	Name	Description	Initial value
15:10	RO	PHY-ID[15:0]	IEEE Address	0x33h
9:4	RO	PHY-ID[15:0]	IEEE Model No.	0x01h
3:0	RO	PHY-ID[15:0]	IEEE Revision No.	0x01h

Note: Register 3 = 0xCC10

4.8.5 Auto Negotiation Advertisement Register of Port0~4

offset : 0x204, 0x224, 0x244, 0x264, 0x284

Bits	Type	Name	Description	Initial value
15	RO	NP	Next Page This bit is defaults to 1, indicating that PHY is next page capable.	0x0h
14	R/W	Reserved	Not Applicable	0x0h
13	RO	RF	Remote Fault 1 – Remote Fault has been detected 0 – No remote fault has been detected This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner.	0x0h
12	RO	Reserved	Not Applicable	0x0h
11	R/W	ASM_DIR	Asymmetric Pause Direction. Bit[11:10] Capability 00 No Pause 01 Symmetric PAUSE 10 Asymmetric PAUSE toward Link Partner 11 Both Symmetric PAUSE and Asymmetric PAUSE toward local device	0x0h
10	R/W	PAUSE	Pause Operation for Full Duplex Value on PAUREC will be stored in this bit during power on reset.	0x1h
9	RO	T4	Technology Ability for 100Base-T4 Defaults to 0.	0x0h
8	R/W	TX_FDX	100Base-TX Full Duplex 1 – Capable of 100M Full duplex operation 0 – Not capable of 100M Full duplex operation	0x1h
7	R/W	TX_HDX	100Base-TX Half Duplex 1 – Capable of 100M operation 0 – Not capable of 100M operation	0x1h
6	R/W	10_FDX	10BASE-T Full Duplex 1 – Capable of 10M Full Duplex operation 0 – Not capable of 10M full duplex operation	0x1h
5	R/W	10_HDX	10Base-T Half Duplex 1 – Capable of 10M operation 0 – Not capable of 10M operation Note that bit 8:5 should be combined with REC100, RECFUL pin input to determine the finalized speed and duplex mode.	0x1h
4:0	RO	Selector Field	These 5 bits are hardwired to 00001b, indicating that the PHY supports IEEE 802.3 CSMA/CD.	0x1h

4.8.6 Auto Negotiation Link Partner Ability Register of Port0~4

offset: 0x205, 0x225, 0x245, 0x265, 0x285

Bits	Type	Name	Description	Initial value
15	RO	NPAGE	Next Page 1 – Capable of next page function 0 – Not capable of next page function	0x0h
14	RO	ACK	Acknowledge 1 – Link Partner acknowledges reception of the ability data word 0 – Not acknowledged	0x0h
13	RO	RF	Remote Fault 1 – Remote Fault has been detected 0 – No remote fault has been detected	0x0h
12	RO	Reserved	Not Applicable	0x0h
11	RO	LP_DIR	Link Partner Asymmetric Pause Direction.	0x0h
10	RO	LP_PAU	Link Partner Pause Capability Value on PAUREC will be stored in this bit during power on reset.	0x0h
9	RO	LP_T4	Link Partner Technology Ability for 100Base-T4 Defaults to 0.	0x0h
8	RO	LP_FDX	100Base-TX Full Duplex 1 – Capable of 100M Full duplex operation 0 – Not capable of 100M Full duplex operation	0x0h
7	RO	LP_HDX	100Base-TX Half Duplex 1 – Capable of 100M operation 0 – Not capable of 100M operation	0x0h
6	RO	LP_F10	10BASE-T Full Duplex 1 – Capable of 10M Full Duplex operation 0 – Not capable of 10M full duplex operation	0x0h
5	RO	LP_H10	10Base-T Half Duplex 1 – Capable of 10M operation 0 – Not capable of 10M operation	0x0h
4:0	RO	Selector Field	Encoding Definitions.	0x01h

4.8.7 Auto Negotiation Expansion Register of Port0~4

offset: 0x206, 0x226, 0x246, 0x266, 0x286

Bits	Type	Name	Description	Initial value
15:5	RO	Reserved	Not Applicable	0x000h
4	RO, LH	PFAULT	Parallel Detection Fault 1 – Fault has been detected 0 – No Fault Detect	0x0h
3	RO	LPNPABLE	Link Partner Next Page Able 1 – Link Partner is next page capable 0 – Link Partner is not next page capable	0x0h
2	RO	NPABLE	Next Page Able Defaults to 1, indicating PHY is next page able.	0x1h
1	RO	PGRCV	Page Received 1 – A new page has been received 0 – No new page has been received	0x0h
0	RO	LPANABLE	Link Partner Auto Negotiation Able 1 – Link Partner is auto negotiable 0 – Link Partner is not auto negotiable	0x0h

4.8.8 Next Page Transmit Register of Port0~4

offset: 0x207, 0x227, 0x247, 0x267, 0x287

Bits	Type	Name	Description	Initial value
15	RO	TNPAGE	Transmit Next Page Transmit Code Word Bit 15	0x0h
14	RO	Reserved	Reserved Transmit Code Word Bit 14	0x0h
13	R/W	TMSG	Transmit Message Page Transmit Code Word Bit 13	0x1h
12	R/W	TACK2	Transmit Acknowledge 2 Transmit Code Word Bit 12	0x0h
11	RO	TTOG	Transmit Toggle Transmit Code Word Bit 11	0x0h
10:0	R/W	TFLD[10:0]	Transmit Message Field Transmit Code Word Bit 10..0	0x001h

4.8.9 Link Partner Next Page Register of Port0~4

offset: 0x208, 0x228, 0x248, 0x268, 0x288

Bits	Type	Name	Description	Initial value
15	RO	PNPAGE	Link Partner Next Page Receive Code Word Bit 15	0x0h
14	RO	PACK	Link Partner Acknowledge Receive Code Word Bit 14	0x0h
13	RO	PMSGP	Link Partner Message Page Receive Code Word Bit 13	0x0h
12	RO	PACK2	Link Partner Acknowledge 2 Receive Code Word Bit 12	0x0h
11	RO	PTOG	Link Partner Toggle Receive Code Word Bit 11	0x0h
10:0	RO	PFLD[10:0]	Link Partner Message Field Receive Code Word Bit 11	0x001h

Chapter 5 Electrical Specification

5.1 TX/FX Interface

5.1.1 TP Interface

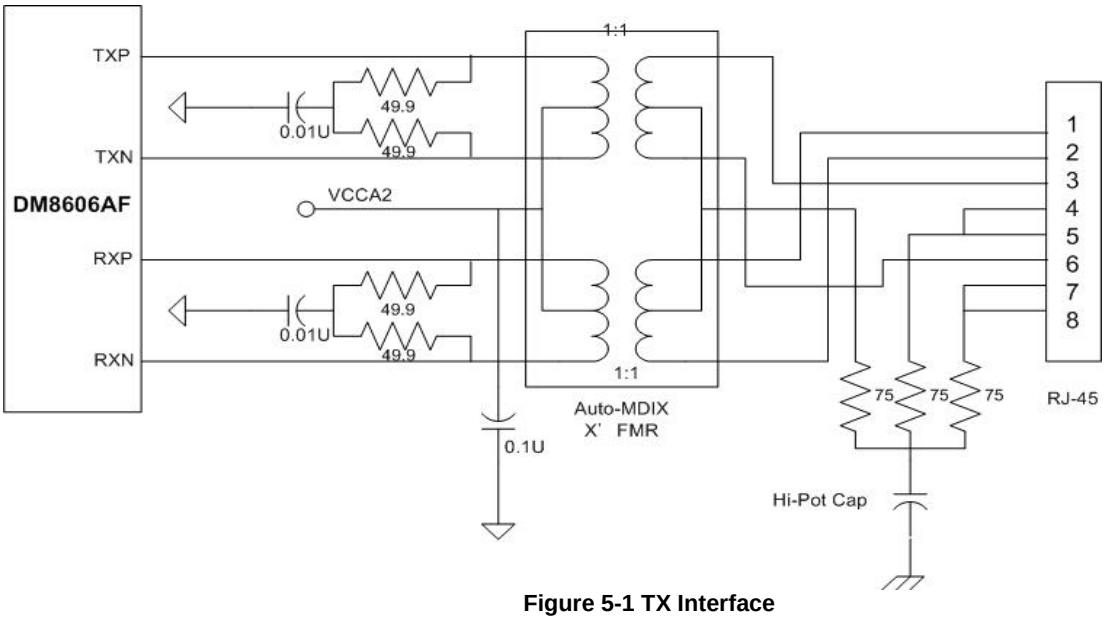


Figure 5-1 TX Interface

Transformer requirement:
. TX/RX rate 1:1
. TX/RX central tap connect together to VCCA2.
User can change TX/RX pin for easy layout but do not change polarity. DM8606AF supports auto polarity on receiving side.

5.1.2 FX Interface

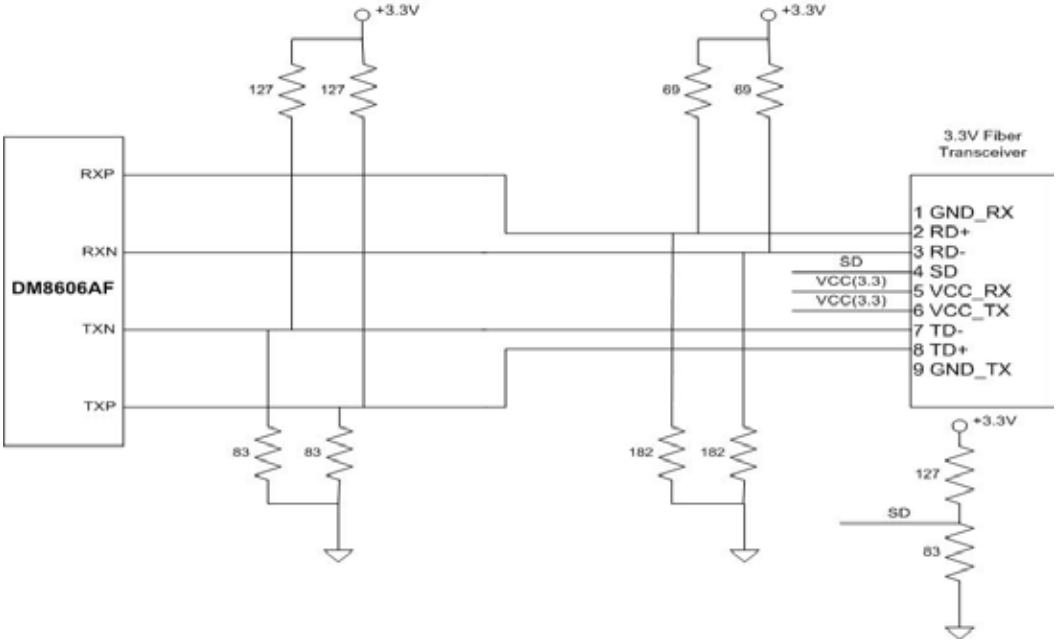


Figure 5-2 FX Interface

5.2 DC Characteristics

5.2.1 Power Consumption

(Under EEPROM Register 0x29 = 0xC000, and 0x30 = 0x0985)

Symbol	Parameter	Rating	Units
P_{100M_5TP}	Power consumption when all twisted pair ports are linked at 100Mbps.	930	mW
P_{10M_5TP}	Power consumption when all twisted pair ports are linked at 10Mbps (include transformer).	1270	mW
P_{DIS_5TP}	Power consumption when all twisted pair ports are disconnected.	450	mW

Table 5-1 Power Consumption

5.2.2 Absolute Maximum Rating

Symbol	Parameter	Rating	Units
V_{CC3O}	3.3V Power Supply for I/O pad	2.97 to 3.63	V
V_{CCBIAS}	3.3V Power Supply for bias circuit	2.97 to 3.63	V
V_{CCAD}	3.3V Power Supply for A/D converter	2.97 to 3.63	V
V_{CCA2}	1.8V Power Supply for line driver	1.62 to 1.98	V
V_{CCPLL}	1.8V Power Supply for PLL	1.62 to 1.98	V
V_{CCIK}	1.8V Power Supply for Digital core	1.62 to 1.98	V
V_{IN}	Input Voltage	-0.3 to V_{CC3O} + 0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC3O} + 0.3	V
$I_{3.3VMAX}$	Maximum current for 3.3V power supply	100	mA
$I_{1.8MAX}$	Maximum current for 1.8V power supply (include transformer)	750	mA
T_{STG}	Storage Temperature	-55 to 155	°C
ESD	ESD Rating	1.5	KV

Table 5-2 Electrical Absolute Maximum Rating

5.2.3 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units
V_{CC3O}	3.3V Power Supply for I/O pad	3.135	3.3	3.465	V
V_{CCBIAS}	3.3V Power Supply for bias circuit	3.135	3.3	3.465	V
V_{CCAD}	3.3V Power Supply for A/D converter	3.135	3.3	3.465	V
V_{CCA2}	1.8V Power Supply for line driver	1.71	1.8	1.89	V
V_{CCPLL}	1.8V Power Supply for PLL	1.71	1.8	1.89	V
V_{CCIK}	1.8V Power Supply for Digital core	1.71	1.8	1.89	V
V_{IN}	Input Voltage	0	-	V_{CC3O}	V
T_J	Junction Operating Temperature	0	25	115	°C

Table 5-3 Recommended Operating Conditions

5.2.4 DC Electrical Characteristics for 3.3V Operation

(Under V_{CC3O}=2.97V ~ 3.63V, T_J= 0°C ~ 115°C)

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IH}	Input High Voltage	TTL	2.0			V
V_{OL}	Output Low Voltage	TTL			0.4	V
V_{OH}	Output High Voltage	TTL	2.4			V
R_I	Input Pull_up/down Resistance	V_{IL}= 0V or V_{IH} = V_{CC3O}		50		KΩ

Table 5-4 DC Electrical Characteristics for 3.3V Operation

5.3 AC Characteristics

5.3.1 XTAL/OSC Timing

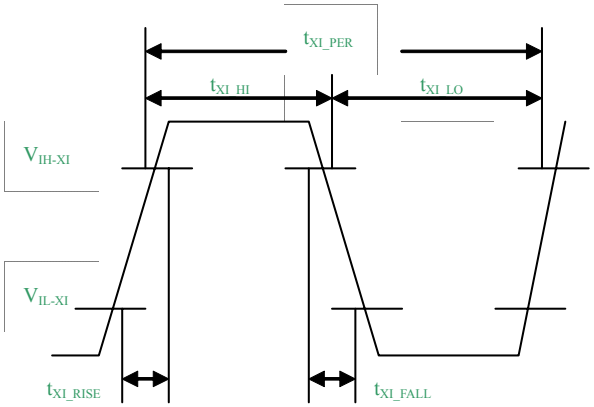


Figure 5-3 XTAL/OSC Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_XI_PER	XI/OSCI Clock Period		40.0 – 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High		14	20.0		ns
T_XI_LO	XI/OSCI Clock Low		14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time , V_{IL} (max) to V_{IH} (min)				4	ns
T_XI_FALL	XI/OSCI Clock Fall Time , V_{IH} (min) to V_{IL} (max)				4	ns

Table 5-5 XTAL/OSC Timing

5.3.2 Power On Reset

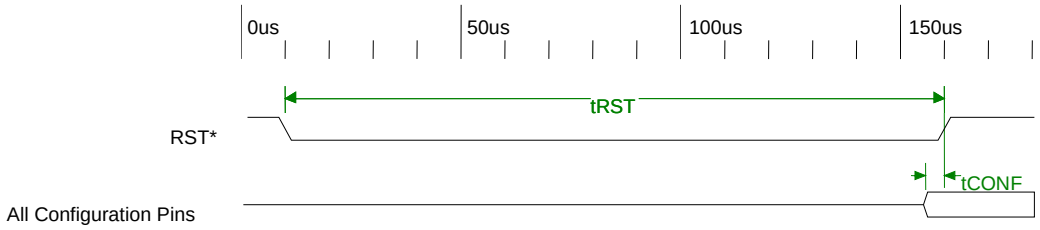


Figure 5-4 Power On Reset Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tRST	RST Low Period		100			ms
tCONF	Start of Idle Pulse Width		100			ns

Table 5-6 Power on reset timing

5.3.3 EEPROM Interface Timing

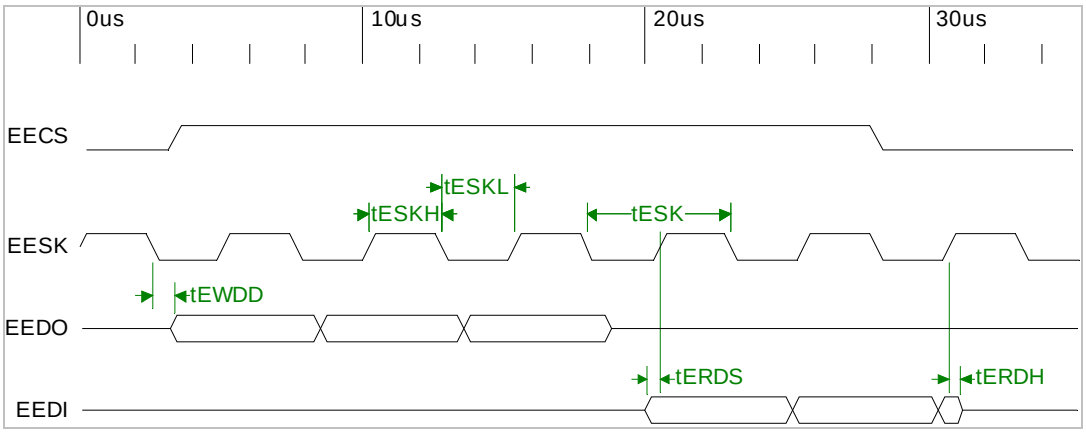


Figure 5-5 EEPROM Interface Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tESK	EESK Period			5120		ns
tESKL	EESK Low Period		2550		2570	ns
tESKH	EESK High Period		2550		2570	ns
tERDS	EEDI to EESK Rising Setup Time		10			ns
tERDH	EEDI to EESK Rising Hold Time		10			ns

tEWDD	EESK Falling to EEDO Output Delay Time				20	ns

Table 5-7 EEPROM Interface Timing

5.3.4 10Base-TX MII Input Timing

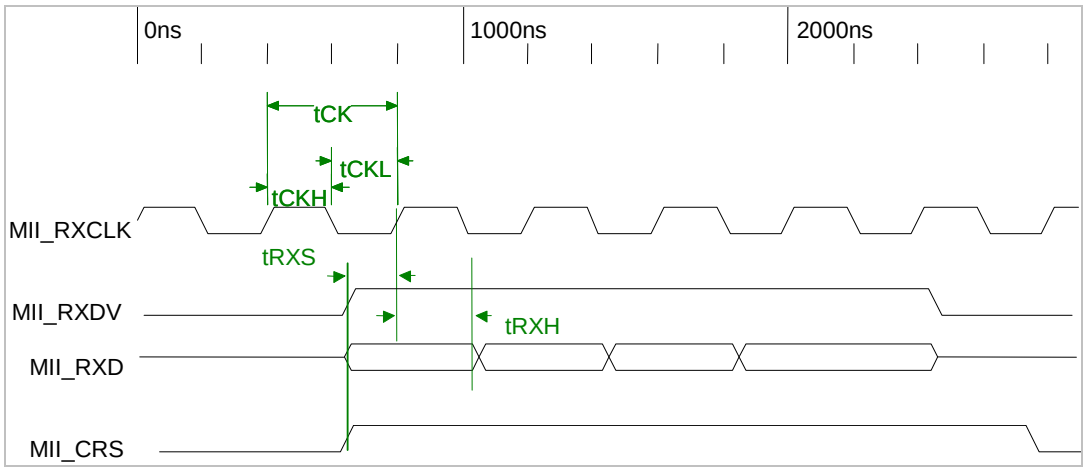


Figure 5-6 10Base-TX MII Input Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_RXCLK Period			400		ns
tCKL	MII_RXCLK Low Period		180		220	ns
tCKH	MII_RXCLK High Period		180		220	ns
tRXS	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup		10			ns
tRXH	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold		10			ns

Table 5-8 10Base-TX MII Input Timing

5.3.5 10Base-TX MII Output Timing

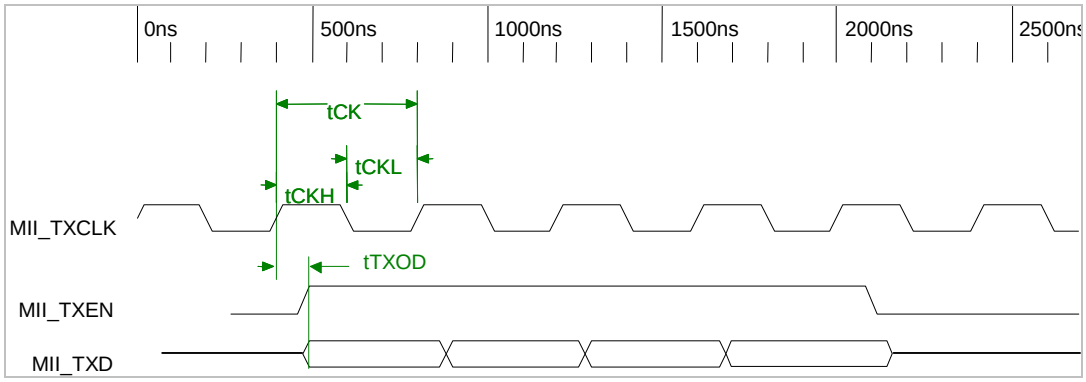


Figure 5-7 10Base-TX MII Output Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_TXCLK Period			400		ns
tCKL	MII_TXCLK Low Period		180		220	ns
tCKH	MII_TXCLK High Period		180		220	ns
tTXOD	MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay		0		25	ns

Table 5-9 10Base-TX MII Output Timing

5.3.6 100Base-TX MII Input Timing

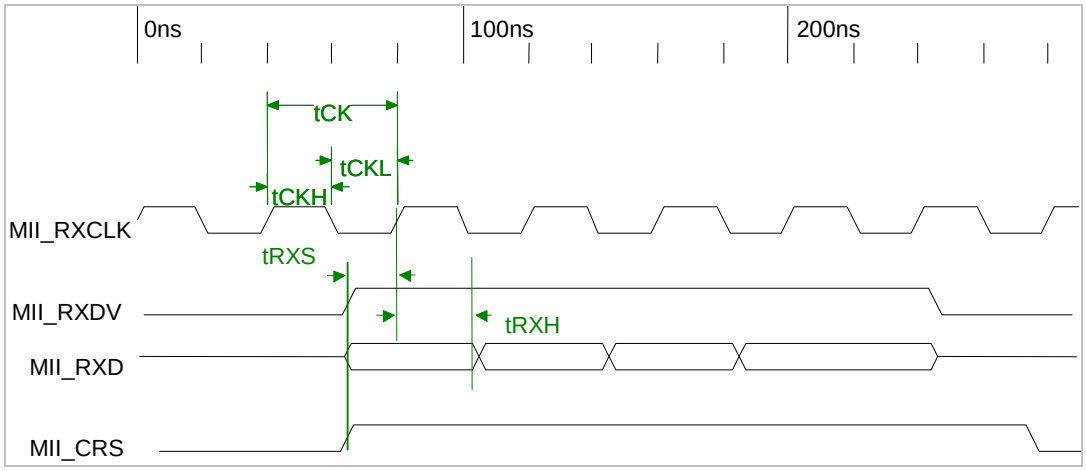


Figure 5-8 100Base-TX MII Input Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_RXCLK Period			40		ns
tCKL	MII_RXCLK Low Period		18		22	ns
tCKH	MII_RXCLK High Period		18		22	ns
tRXS	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup		10			ns
tRXH	MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold		10			ns

Table 5-10 100Base-TX MII Input Timing

5.3.7 100Base-TX MII Output Timing

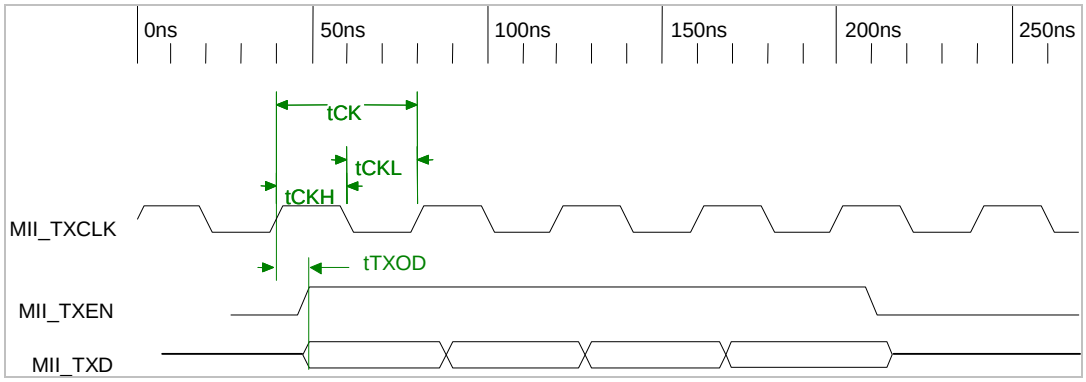


Figure 5-9 100Base-TX MII Output Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
tCK	MII_TXCLK Period			40		ns
tCKL	MII_TXCLK Low Period		18		22	ns
tCKH	MII_TXCLK High Period		18		22	ns
tTXOD	MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay		0		25	ns

Table 5-11 100Base-TX MII Output Timing

5.3.8 GPSI (7-wire) Input Timing

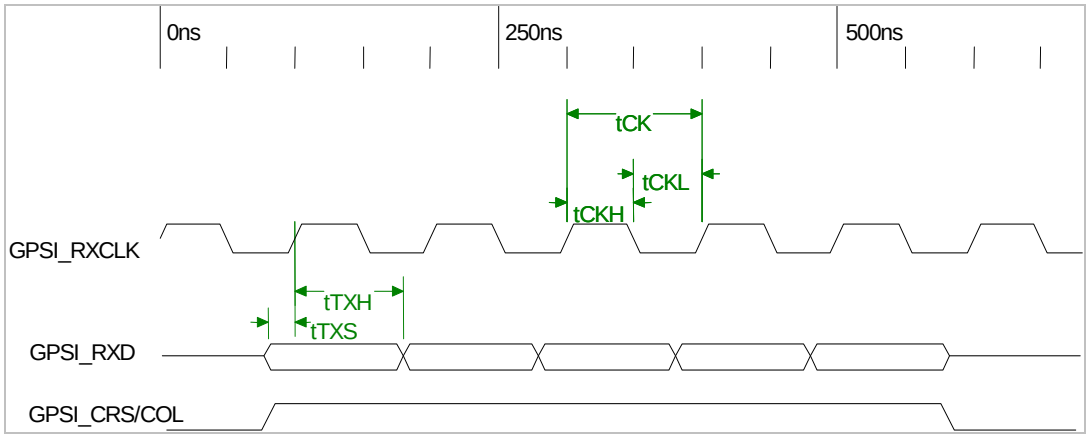


Figure 5-10 GPSI (7-wire) Input Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
TCK	GPSI_RXCLK Period			100		ns
TCKL	GPSI_RXCLK Low Period		40		60	ns
TCKH	GPSI_RXCLK High Period		40		60	ns
TTXS	GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising Setup Time		10			ns
TTXH	GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising Hold Time		10			ns

Table 5-12 GPSI (7-wire) Input Timing

5.3.9 GPSI (7-wire) Output Timing

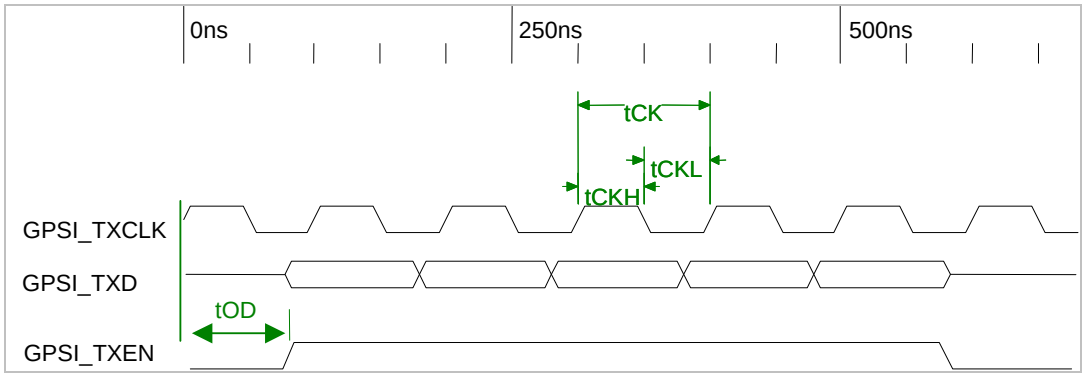


Figure 5-11 GPSI (7-wire) Output Timing

Symbol	Parameter	Conditions	Min	Typical	Max	Units
TCK	GPSI_TXCLK Period			100		ns
TCKL	GPSI_TXCLK Low Period		40		60	ns
TCKH	GPSI_TXCLK High Period		40		60	ns
TOD	GPSI_TXCLK Rising to GPSI_TXEN/GPSI_TXD Output Delay		50		70	ns

Table 5-13 GPSI (7-wire) Output Timing

5.3.10 SDC/SDIO Timing

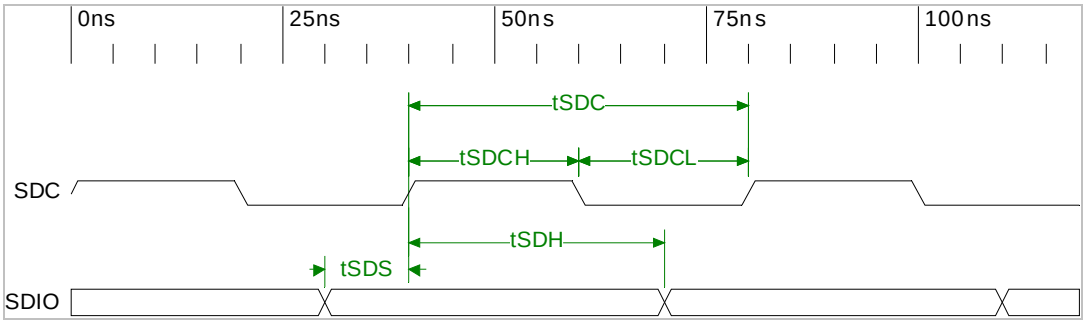


Figure 5-12 SDC/SDIO Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	SDC Period		20			ns
TCKL	SDC Low Period		10			ns
TCKH	SDC High Period		10			ns
TSDS	SDIO to SDC rising setup time on read/write cycle		4			ns
TSDH	SDIO to SDC rising hold time on read/write cycle		2			ns

Table 5-14 SDC/SDIO Timing

5.3.11 MDC/MDIO Timing

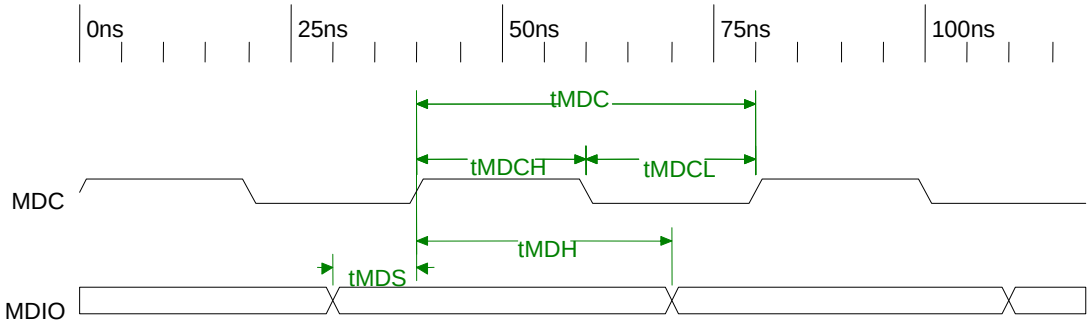


Figure 5-13 MDC/MDIO Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tMDC	MDC Period		100			ns
tMDCL	MDC Low Period		40			ns
tMDCH	MDC High Period		40			ns
TMDS	MDIO to MDC rising setup time on read/write cycle				10	ns
TMDH	MDIO to MDC rising hold time on read/write cycle		10			ns

Table 5-15 MDC/MDIO Timing

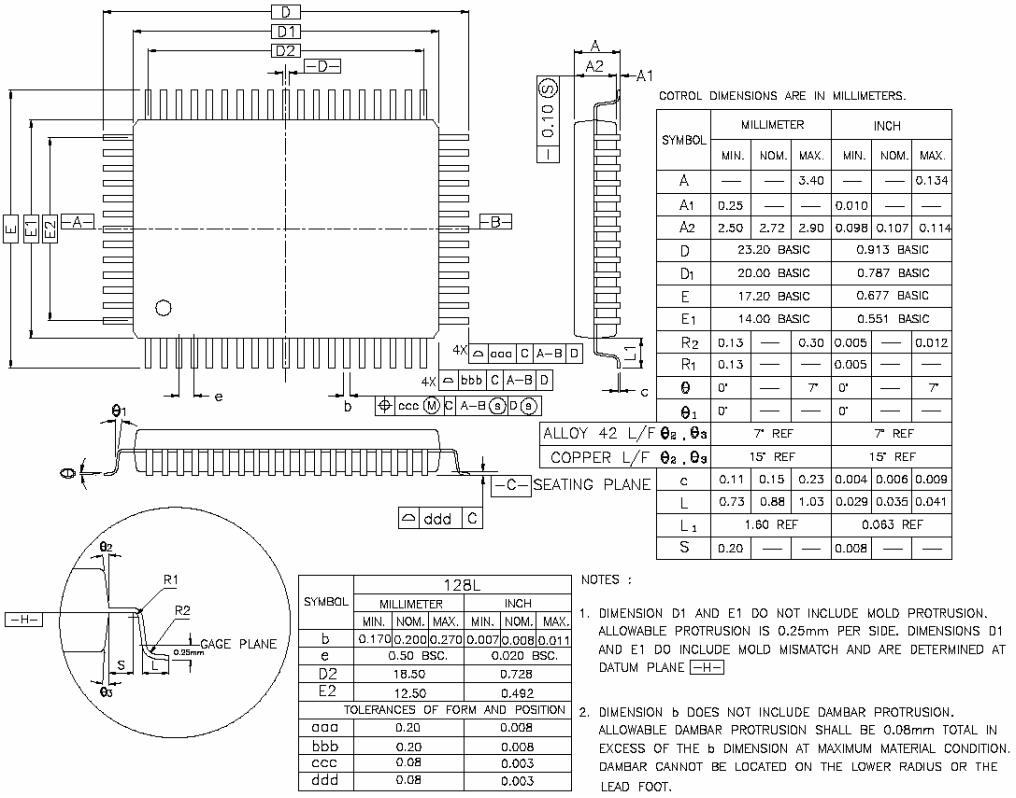
5.3.12 Magnetics Selection Guide

Refer to Table for transformer requirements. Transformers, meeting these requirements, are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table are electrical equivalents, but may not be pin-to-pin equivalents

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1078, H1012, H1102
Delta	LF8200, LF8221x
YCL	20PMT04, 20PMT05, PH163112 , YCL 0303 PH163539 *(Auto MDIX), PTC1411-00N
MAGCOM	HS4012 , HS9001 , HS9016
Halo	TG22-3506ND, TD22-3506G1, TG22-S010ND, TG22-S012ND TG110-S050N2
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37 NPI 6170-30
Fil-Mag	PT41715
Bel Fuse	S558-5999-01, S558-5999-W2
Valor	ST6114, ST6118
Macronics	HS2123, HS2213
Bothhand	TS6121C,16ST8515,16ST1086
SUMLINK	ST-L1164,ST-L1105

Chapter 6 Packaging and Ordering

128 Pin QFP Outside Dimension



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2, θ3	7° REF			7° REF		
COPPER L/F θ2, θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

Figure 6-6-1 128 Pin QFP Outside Dimension

Ordering Information

Part Number	Pin Count	Package
DM8606AF	128	QFP
DM8606AFP	128	QFP (Pb-Free)

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.